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OVERVIEW OF EUROPEAN TECHNOLOGY IN COMPUTERS, TELECOMMUNICATIONS, AND ELECTRONICS

a report

by J.F. Blackburn

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The emergence of the personal computer, the growing use of distributed systems, and the increasing demand for supercomputers and minisupercomputers are causing a profound impact on the European computer market. Microelectronics (the microchip) is the driving force for developments in both computers and telecommunications and is the factor that has led to their merging. The European Community is concentrating on R&D in computers, telecommunications, and electronics; it is also driving forward toward standardization. Another important consideration in Europe is the speed with which Europe follows the U.S. example toward privatizing and liberalizing the public telecommunications service.

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This special issue of ESNIB is devoted to Dr. J.F. Blackburn. Dr. Blackburn is the London representative of the Commerce Department for Industrial Assessment in Computer Science and Telecommunications.

OVERVIEW OF EUROPEAN TECHNOLOGY IN COMPUTERS, TELECOMMUNICATIONS, AND ELECTRONICS . . . . . J.F. Blackburn

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Overview of European Technology in Computers, Telecommunications, and Electronics

by J.F. Blackburn. Dr. Blackburn is the London representative of the Commerce Department for Industrial Assessment in Computer Science and Telecommunications.

Executive Summary

The emergence of the personal computer, the growing use of distributed systems, and the increasing demand for supercomputers and minisupercomputers are causing a profound impact on the European computer market. An equally profound development in telecommunications is the integration of voice, data, and images in the public network systems--the Integrated Services Digital Network (ISDN). This integration is made possible by higher-speed transmission and switching systems and by the digitalizing of signals in all kinds of information. Microelectronics (the microchip) is indeed the driving force for developments in both computers and telecommunications and is the factor that has led to their merging.

The heaviest concentration of research and development (R&D) in the European Community (EC) is in computers, telecommunications, and electronics. European Strategic Programme for Research Development in Information Technologies (ESPRIT), a 3.2 billion European Currency Unit (ECU) program, is just starting its second 5-year phase. Research and Development in Advanced Communications Technologies in Europe (RACE), a 550-million ECU program, began its 5-year phase in 1988, and will concentrate on the R&D required for broadband ISDN to be introduced throughout Europe by 1995. The European Research Coordination Agency (EUREKA) is not EC-sponsored, but the EC as a whole and all its individual members (as well as a half dozen other European countries) are participating in it. With its main emphasis on information technology (IT) (about 25 percent of its total), the EUREKA program covers a wide range of high-technology fields. Beginning in 1989, Basic Research in Industrial Technologies for Europe/European Research on Advanced Materials (BRITE/EURAM) combines the BRITE and EURAM programs into one coordinated program. The program will concentrate on advanced materials technologies and technologies for the manufacturing industry and has a budget of 440 million ECU for 5 years. Apart from Europe-wide programs, the national programs on R&D are concentrating on much the same three main areas--computers, telecommunications, and electronics. Examples in the U.K. are the Joint Optoelectronic Research Scheme (JOERS) for optoelectronics, the LINK program to stimulate collaboration between industry and universities, the Alvey Program of research in IT, and the efforts to stimulate the use of the transputer for engineering and science. Of course, the U.K. is a major participant in the EC programs and, for example, the U.K. has contributed £200 million to ESPRIT II.

An excellent example in the Federal Republic of Germany (FRG) is the government-sponsored SUPRENUM program to develop a super computer with a performance reaching 5 Gigaflops. Also, the megaproject of Siemens and Philips, with some government help, is producing 4-megabit chips and will proceed to 16-megabit chips and beyond at a later date. The megaproject has now been included as the base on which to proceed with the Joint European Submicron Silicon Initiative (JESSI) program (see page 24). Like the U.K., the FRG participates substantially in the EC programs.

In France and Italy, and indeed in most other European countries, there is substantial emphasis on R&D in microelectronics, IT, and telecommunications. These are the industries in which Europeans believe they must achieve comparability with the U.S. and Japan.

The other important consideration in Europe is the speed with which Europe follows the U.S. example toward privatizing and liberalizing the public telecommunications service. In this matter, the U.K. has been the leading mover. In 1984, British Telecom, then the sole provider of basic telecommunications service, became a private company. Both

British Telecom and Mercury, a subsidiary of Cable and Wireless Company, now provide basic telecommunications service competitively. The customer premises equipment market and the value-added network (VAN) services market are free markets in principle. However, equipment and services must pass acceptance tests.

In no other country have matters moved so rapidly; however, the trend in this direction continues all over Europe. As of January 1, 1989, the Netherlands Postal Telephone and Telegraph became a private company, though government owned. Its employees are not civil servants and the company can make a profit and acquire financing on the financial market. Customer premises equipment and value-added services will be obtained competitively. Similarly, in Spain, an Omnibus Telecommunications Law came into effect January 1989, similar to that in the Netherlands. In the FRG, Telekom is now a government-owned private company as of January 1990 and provides basic telecommunications services.

Before 1990 in the FRG, the Federal Ministry of Posts and Telecommunications had four main operating divisions--postal services, postal banking services, and two divisions concerned with telecommunications. As of the beginning of 1990, a postal services company, a postal banking services company, and a telecommunications company (Telekom), comprising two telecommunications divisions, are wholly government owned. The companies operate like private companies with profit/loss responsibility and can borrow money on financial markets. Competition is allowed in customer premises equipment such as terminals, telephones, and private base-exchange PBXs as well as VAN services. However, Telekom, still monopolizes the telecommunications network. This is conditional that private service companies will be assigned leased transmission lines appropriately and competitively.

The telephone service, as the pure transmission of the spoken language, will remain a state monopoly, but not the combined services with text, picture, or data which also includes articulation. Consequently, a further reduction in state monopoly will come with the introduction of new telecommunications services, which also includes articulation.

France, Italy, Sweden, Switzerland, Belgium, and others have made small moves in the direction of liberalizing their telecommunications market. Most countries are moving in the direction recommended by the EC--liberalizing the market for customer premises equipment and VAN services.

The EC is driving forward toward standardization. This is particularly important in the telecommunication industry, in order that equipment manufactured in one European country can be operated in another with little or no modification. Standardization requires product standards and a common system of acceptance tests. Open Systems Interconnection (OSI) is the objective for the European telecommunication service.

Standards in the computer field are also under serious pressure. This results, also in part, from the growing use of distributed systems and the resulting need for compatibility between systems from different manufacturers. Manufacturers in Europe and the U.S. are striving to achieve intercommunication and even interoperation among systems from different manufacturers.

In the main body of this report more detail is given on various research programs in computers, microelectronics, and communications. In the computer research area, emphasis has been on the massively parallel concept for supercomputers. The only serious effort in Europe to develop a vector processor system was by the Bull company in France. Although fully developed, a decision was made not to market this product. The single most important development to date was the transputer, developed by Inmos in the U.K., a microprocessor that has served as the basis for products now marketed by Meiko and Parsys in the U.K., Parsytec in FRG, and Telmat in France. The other significant, though less important development, was the Suprenum project in FRG. This massively parallel processor will be marketed by a new company called Suprenum. The Genesis project in the ESPRIT II program is in the very early stages of development and will combine the resources of Suprenum, Bull, Inmos and Siemens. Genesis' objective is to develop a family of supercomputers, and the architecture will almost certainly be based on a massively parallel system.

The significant effort in microelectronics, apart from the Inmos development of the transputer, is the Joint European Submicron Silicon Initiative (JESSI). This program starts from the base of the Mega project of Siemens and Philips, in which they developed and are marketing 4 Mbit Dynamic Random Access Memory (DRAM) chips. The JESSI program has added SGS-Thomson, and recently IBM, and has as an objective the development of 0.3 micron feature size chips capable of storing 64 megabits of information.

There are two highly significant programs in communications. The RACE program of the European Commission has, as a single objective, the development of all the technology needed for an integrated broadband communications (IBC) system for the mid 1990s. This program will incorporate integrated services digital network (ISDN) technology. The other highly important program is the high-definition television (HDTV) project under the EUREKA program. This project has already developed and demonstrated a pilot model of a 50 cycle, 1250-line, high-definition system (*ESNIB* 90-03:24-32).

Market Assessment Summary

The U.S. remains the principal supplier of computers and peripheral equipment in Europe--a market of about $85 billion/year. However, the growth in turnover, expressed as a percentage of turnover per year, averaged over 1984-1987, favors European suppliers in growth--Nixdorf, Olivetti, and Philips were the top three.

Notably, several new computer companies in Europe are successfully marketing massively parallel systems based on the transputer developed by Inmos of Bristol. Inmos was bought early in 1989 by SGS-Thomson, the Italian-French microelectronics company. Together, Meiko and Parsis of the U.K., Telmat of France, and Parsytec of the Federal Republic of Germany, have sold about 500 systems over the past 2 years. These systems have ranged in size from 16 to 400 transputer systems.

In telecommunications, with the sale of ITT's telecommunications business to Alcatel of France, the U.S. role in European telecommunications was greatly diminished. However, AT&T has formed alliances of various sorts with Philips of the Netherlands and with Olivetti and Italtel of Italy and has established a presence in these and several other European countries. Also, U.S. operating companies are successfully selling software and expertise in operations in Europe.

U.S. microelectronics companies now share about equally with European manufacturers some 80 percent of the European microelectronics market. Japan has about 19 percent of that market. However, after the European Single Market comes into effect in 1992, it will become more essential for products sold in Europe to have been manufactured in Europe. This means that American companies must increase their European production facilities in order to retain market share.

In all of these markets, it will be very important for U.S. companies to have early information on standards and other plans for products to be marketed in Europe. The best way to get timely information is through participation in the planning and developing process for products. Thus, it would be highly desirable to have some American participation in such European programs as the Joint European Submicron Silicon Initiative (JESSI) and the High-Definition Television (HDTV). This would, of course, require reciprocity through European participation in comparable work in Microelectronics and Computer Technology Corporation and Sematech.

Two important announcements in the first quarter of 1990 concerning HDTV and the JESSI programs were:

- NBC, a division of RCA Corporation, and Thomson Consumer Electronics announced that they would joint with North American Philips Corporation on HDTV development
- On March 5, 1990, the London INDEPENDENT carried the story that IBM is to join the JESSI program (see page 24). An earlier announcement had reported that IBM and Siemens would work together to develop and produce 64M-bit DRAMs. The other major partners in JESSI are Siemens, Philips, and SGS-Thomson.

Chapter I - Europe

Europe-Wide Trends and Actions

Computers

The three most important trends in the computer field in Europe, and indeed world-wide, are the emergence of the personal computer (PC), the trend toward distributed systems, and the growth in demand for supercomputers and minisupercomputers.

Personal Computers

There has been enormous growth in the market for PCs since their introduction in the late 1970s and early 1980s. In the U.S., more than 14 million office PCs are in use, and more than 5 million in Europe. However, the market in Europe is expected to grow more rapidly than the market in the U.S. By 1992, the forecast is that European market will be more than 50 percent of the U.S. market. In Europe, the four largest suppliers of PCs and each supplier's percentage of the European market are IBM - about 25 percent, Olivetti - about 11 percent, Apple - about 7 percent, and Commodore - about 4 percent.

There are several reasons for the rapid growth of the professional PC market in Europe (see Table 1).

Table 1. European PC Market Growth

Reduction in price. The price has dropped more than 50 percent over the last 3 years.
Increased acceptance in large accounts. This has been especially pronounced in the U.K. and Germany.
Increased computer literacy. Young graduates entering the work force have often been trained on PCs at school.
Availability of software packages in local language. For example Lotus, Wordstar, and Multimate are available in most European languages.

Besides the four leaders mentioned above, other vendors are Victor, Bull, Hewlett-Packard, Amstrad, Tandon, Zenith, and Compaq. In addition, nearly 6 percent of the European market is met by Southeast Asia (SEA) clones. The SEA clones come into Europe through large distribution organizations like Migros in Switzerland and through small importers that trade in cheap clones. About one third of the PCs sold in Europe are sold through dealer or distribution channels and this trend is expected to continue. There are about 8,500 dedicated PC vendors in Europe.

Several developments that are now occurring will provide further impetus to growth in the PC market. A factor (see Distributed Computer Systems), is the growing importance of networks and distributed computing. The number of PCs serving as workstations on distributed computer networks is greatly increasing. Individual users will have access to shared databases and other outside information and facilities. Another factor will be the integration of work group productivity applications and artificial intelligence (AI) methods.

Distributed Computer Systems

The importance of distributed computers over a communications network and interoperability of different computers in the system is very well illustrated by the remarkable growth of the Digital Equipment Corporation (Digital) over

the past several years. This trend has greatly stimulated the market for minicomputers, PCs, and workstations. Digital is a major supplier of minicomputers and workstations. In Europe, four companies account for about 90 percent of the workstation market--SUN, Apollo, Hewlett-Packard, and Digital. In the U.K., ICL markets SUN workstations; in the Federal Republic of Germany (FRG), Siemens markets Apollo workstations. However, in the first quarter of 1990, IBM added the Reduced Instruction Set Computer (RISC) System/6000 workstation to its product line. This had an almost immediate sales impact.

As mentioned above, the growing importance of distributed computing and computer networks has and continues to stimulate the PC market. The PCs are also used as workstations on networks. In a truly distributed computing system with hierarchical control over a collection of processors (workstations, PCs, minicomputers), the user specifies the work to be done and the control system allocates the work to the appropriate computing resource in the system.

From 1978 through 1984 in the U.K., Science and Engineering Research Council (SERC) funded a study of theory, methodology, and resource management in a distributed computing system. The major research areas covered were theory and languages; resource management; architecture; operational attributes; and design, implementation, and application. Some of the results were reported in a NATO workshop held in October 1982 (see *ESN* 36-12:325-331), along with work in France and the FRG. Professor B. Randell, University of Newcastle, U.K., described some of the work done on operational attributes. The system employs the component design principle and the UNIX system as a basic component. A system called the Newcastle Connection was designed and implemented for uniting multiple UNIX systems. The resultant system is called UNIX United. Functions such as file access, device access, and input/output control work across multiple machines. Issues of interprocessor communications and network protocols are hidden from the user. All existing programs using multiple processors can be run in the system. A user does not need to know on what machines his program is run. A successor to the Newcastle Connection is in regular use at Newcastle.

Supercomputers

Between 1984 and 1989, the number of supercomputers in Europe grew by a factor of 5. Table 2 gives the distribution by manufacturer in 1989, but does not include minisupercomputers like the Alliant, Convex, SCS, and FPS machines.

Table 2. Supercomputer Distribution in Europe in 1989

Manufacturer	Machine	Number of Installations Type	Total
Cray	Cray 2	8	
	Cray XMP	42	
	Cray YMP	10	
	Cray 1	6	66
Fujitsu	Amdahl Version	7	
	Siemens Version	10	17
CDC	Cyber 205	2	2
IBM (estimated)	390 + Vector Function	125	125
NEC	SX-2	1	1
	TOTAL		211

The distribution of supercomputers by country is provided in Tables 3 through 6. However, sensitive sites and IBM installations are not included; IBM does not disclose information on their sites, thus the figure of 125 shown in Table 2 is only an estimate. However, IBM is encouraging the growth of vector computing by supporting several centers in the public sector including RAL (U.K.), CERN (Switzerland), Aachen (FRG), and CNUSC (France). There are two major IBM research centers in Europe with IBM 390 + Vector installed--The Bergen (Norway) Scientific Centre with an IBM 3090/200VF and ECSEC Center in Rome with the IBM 390/600VF. Table 6A gives distribution by country of IBM 3090/VF installations in Europe.

At a 5-day conference held in Tromsø, Norway, in June 1988, the changing role of supercomputers was extensively discussed (ONREUR Report 9-1-C). The keynote speaker, Alan Weis, Vice President, IBM, Data Systems Division, said that users are moving toward the supercomputer because it is becoming widely recognized by government, industry,

and universities as a useful and more available tool for solving problems requiring a large quantity of data and very fast computation. New applications requiring extensive computation are bringing increased demand for supercomputers; e.g., the use of fractals for various problems in physics and engineering and the use of finite elements in fuselage design in the aeronautics industry. The environment for using the supercomputer is now better understood and the requirements for the applications are being better addressed; e.g., X-windows on a vector computer. Scientists can observe and steer processes and *fly* over a silicon chip for more information on chemical bonds through changing the current applied to the materials.

Table 3. Summary of Supercomputers in the U.K.

Institute	Location	Supercomputer
Atomic Weapons Research Establishment (AWRE)	Aldermaston	Cray 1S Cray X-MP/28 Cray Y-MP8/832 on order
British Aerospace		Cray Y-MP 2/132
British Petroleum Exploration	London	Cray X-MP/24
Cray Research (U.K.)	Bracknell	Cray X-MP/216
European Centre for Meteorology & Weather Forecasting (ECMWF)	Reading	Cray Y-MP8/864
General Electric Company (GECO)	London	Amdahl VP 1100 & 1100E
Harwell Laboratory	Didcot	Cray 2
Merlin Profilers Ltd	Woking	Cray 1S
Royal Aircraft Establishment (RAE)	Farnborough	Cray 2
Rutherford Appleton Laboratory (RAL)	Chilton	Cray X-MP/416
Royal Armament Research and Development (RARDE)	Fort Halstead	Cray 1S
Shell	Wythenshaw	Cray X-MP/216
U.K. Meteorology	Bracknell	Cray Y-MP8/832
University of London Computing Centre (ULCC)	London	Cray X-MP/28
University of Manchester Computing Centre (UMCC)	Manchester	Amdahl VP 1200 Amdahl VP 1100
Western Geophysical	London	Amdahl VP 1200

Table 4. Summary of Supercomputers in France

Institute	Location	Supercomputer
Aerospatial	Toulouse	Cray X-MPE/116se
Ecole Polytechnique	Palaiseau	Cray 2
Commission d'Energie Atomique (CEA)	Cadarache Limeil Saclay Vaujours	Cray X-MP/14se Cray X-MP/416 Cray 1S Cray X-MP/28 Cray 1S
Centre European de Recherche Avance en Calcul Scientifique (CERFACS)	Toulouse	Cray 2
Centre Interregionale de Calcul Electronique (CIRCE)	Orsay	Siemens VP 200
Centre Interregionale de Service en Informatique (CISI)-Framatome	Gir-sur-Yvette	Cray X-MP/416
Citroen/Puegeot PSA	Neuilly-sur-Seine	Cray X-MP/216
Compagnie Generale Geophysique (CGG)	Massy	Cray X-MP/24
Electricite de France (EDF) Clamart		 Cray Y-MP8/432 Cray Y-MP4/232
Michelin	Clermont Ferrand	Cray X-MP/14se
Office Nationale d'Etudes et de Recherche Aerospatials (ONERA)	Chatillon	Cray X-MP/116
Petroleum Research Elf Aquitaine	Pau	Cray X-MP/12
Petroleun Research Total	Paris	Cray X-MP/24 Cray X-MP/24
Renault	Rueil Malmaison	Cray X-MP/18

Table 5. Summary of Supercomputers in the Federal Republic of Germany

Institute	Location	Supercomputer
Technical University, Aachen	Aachen	Siemens VP 200
Adam Opel	Russelsheim	Cray X-MP/14
Bavarian Motor Works (BMW)	Munich	Cray X-MP/28
Ruhr University, Bochum	Bochum	Cyber 205
Daimler-Benz	Stuttgart	Cray X-MP/24
Deutsch Forschungs und Versuchs Anstalt für Luft und RaumFahrt (DFVLR)	Oberfaffenhofen	Cray X-MP/216
DKRZ, Nuclear Research	Hamburg	Cray 2
HLRZ, High Level Computing Center	Julich	Cray Y-MP8/832
Industrieanlagen Betriebs Gesellschaft (IABG)	Ottobrun	Siemens VP 200
Universitat Kaiserlautern	Kaiserlauten	Siemens VP 100
Universitat Karlsruhe	Karlsruhe	Siemens VP 400-EX
Kernforschungsalange (KFA) Julich (Nuclear)	Julich	Cray X-MP/416
Kernforschung Zentrum (KFK) Karlsruhe (Nuclear)	Karlsruhe	Siemens VP 50-EX
Universitat Kiel	Kiel	Cray X-MP/216
Liebniz Rechenzentrum	Munich	Cray Y-MP4/432
Max Planck Institut	Garching Hamburg	Cray X-MP/216 Cyber 205
Prakla-Siesmos	Hannover	Cray X-MP/18
Siemens AG	Munich	Siemens VP 200 Siemens VP 160-EX
Universitat Stuttgart	Stuttgart	Cray 2
Volkswagen (VW)	Wolfsburg	Cray X-MP/28
Wetter Dienst	Offenbach	Cray Y-MP4/432
Continental AG	Hannover	Cray X-MP 18se
RRZN (Super Computer Center)	Hannover	Siemens VP 200-EX
Zuse Institute, Berlin (ZIB)	Berlin	Cray X-MP/24

Table 6. Summary of Supercomputers in Other European Countries

Country	Institute	Location	Supercomputer
Austria	Vienna University	Vienna	Siemens VP 50-EX
Belgium	Brussels University	Brussels	Cray X-MP/14
	Antwerp University	Antwerp	ETA 10P
Denmark	UNI*C (University)	Lyngby	Amdahl VP1100
Finland	VTKK (University)	Espoo	Cray X-MP/EA/416
Italy	Computing Center for Supercomputers (CINECA)	Bologna	Cray Y-MP8/432
	ENEL (Italian National Agency for Electricity)	Pisa	Cray X-MP/14
	Fiat	Torina	Cray X-MP/14se
	Trieste University	Trieste	Cray X-MP/14
Netherlands	ENR, Petroleum R&D KSEPL,	Petten	ETA 100
	Petroleum R&D NLR, Petroleum	Rijswijk	Cray X-MP/164
	R&D Stichting Academisch Rekencentrum, (Consortium of Universities)	Petten	NEC SX2
Norway	General Electric Co. (GECO)	Stavenger	Amdahl VP 1100
	Norcomp, Oil Research	Nortodden	Amdahl VP 1100
	RUNIT, Oil Research	Trondheim	Cray X-MP/28
Spain	CASA, Aeronautical Engineering	Madrid	Cray X-MP/14se
	Tecnatom	Madrid	Cray X-MP/14
Sweden	SAAB-Scania	Linkoping	Cray 1S Cray X-MP/48
Switzerland	CERN, Atomic Energy Research	Geneva	Cray X-MP/48
	Ecole Polytechnique Federal (EPFL)	Lausanne	Cray 2 (2 pr)
	Swiss Federal Institute of Technology (ETH)	Zurich	Cray X-MP/28

Table 6A. Summary of IBM 3090/VF Installations in Europe

Austria	3
Belgium	5
Britain	13
Denmark	2
Finland	2
France	29
Germany	25
Italy	24
Netherlands	4
Norway	2
Spain	4
Sweden	4
Switzerland	7
Turkey	1
TOTAL	125

Alan Erisman, Boeing Computer Services, said that some successes because of supercomputers have occurred in understanding molecular structure and fluid flow under various conditions. Successes in product development include the design of Boeing 738-3000 and the Ford Taurus. Enhanced oil recovery is another area where using supercomputers is important.

Most supercomputers in use today are of the coarse-grained variety in which parallel processing with up to six powerful vector processors work in parallel. This is true of Cray and Fujitsu machines, and IBM's 3090VP systems. An evolutionary approach has been taken by IBM to parallel processing going back to the 1960s when the 360/50 was used as an attached support processor, together with larger 360 machines like the 360/65 or 360/85. This evolution has progressed to the present six-processor 3090VP with six attached vector processors. This evolutionary approach has allowed IBM customers to avoid massive reprograming as they moved to more powerful systems.

Gene Amdahl, founder of Amdahl Corporation, says that multiple processing architectures are not extendable without limit. He stated that even in circumstances where software can be split into 100 separate programs, each capable of parallel execution, there is little worthwhile increase in performance in parallel processing systems above 18 processors. While it does not appear that the manufacturers of big vector processors are planning in the near term beyond the limit that Amdahl suggested, other manufacturers are proceeding with fine-grained systems in which hundreds or thousands of rather simpler processors work in parallel.

The Meiko Company, Bristol, U.K., is a European-developed example that markets the Meiko Multiple Computing Surface (MMCS) based on the transputer developed by Inmos, Bristol. The transputer and MMCS have been subjects for many *ESN* articles (see *ESN* 40-9:306-308; *ESN* 40-4:142; *ESNIB* 88-01:29-31; *ESNIB* 88-02:30-33; *ESNIB* 88-03:33-40). Briefly, the T800 transputer is a 32-bit complementary (symmetry) metal oxide semiconductor (CMOS) microcomputer with a 64-bit floating point unit and graphics support. The T800 transputer has 4k bytes of random access memory (RAM) on chip for high-speed processing, a configurable memory interface, and four standard Inmos communications links.

The MMCS is a highly parallel, flexible, and extensible concurrent supercomputer; it is composed of modular subsystems that permit optimization of the commands *compute*, *store*, and *input/output* to particular classes of applications. The MMCS was ready for general release by summer 1986 and by the end of 1989, about 300 systems had been sold. Parsytec, FRG, also markets transputer-based parallel systems. Most systems delivered are too small to be classified as supercomputer. However, the system being installed at the Edinburgh Concurrent Supercomputer Center will certainly be a supercomputer when the number of processors reaches the expected 1,000 (see *ESNIB* 88-03:35-40). As of the end of 1989, this system had 400 processors. Several other systems under development are based on the transputer and will be discussed later.

Telecommunications

As the European countries move toward their big objective for the next decade, the introduction of an Integrated Services Digital Network (ISDN), and along with the Open Systems Interconnection (OSI) in their public network, an enormous increase in research and development (R&D) is taking place. This R&D will be discussed in subsequent sections devoted to the ESPRIT, RACE, EUREKA, and BRITE programs.

The practical implications of the technological change resulting from ISDN and OSI will affect the manufacturers of computers and telecommunications equipment, users of the telecommunications and computers, and especially the operators of the public networks in all of the European countries. Several communications and computing equipment manufacturers are offering, or will offer, value-added network (VAN) services that go beyond transmitting and switching and include computer processing of the information being transmitted.

In European countries, the traditional system of providing telecommunications service has been through a government-owned and -controlled monopoly system. As computing (traditionally a nonmonopoly) converges with communications (traditionally a monopoly) it is becoming increasingly difficult to draw the line between the monopoly and the nonmonopoly. This issue becomes more complicated with the growing business of value-added services combined with communications. Different European countries are reacting in different ways to this new situation resulting from technological change.

All European countries are facing the problem of providing new regulations to cover the rapidly changing situation. A policy that allows smaller competitors to come into the market should not be too restraining on the dominant operator. Promoting competition within a country should not be at the expense of loss of competitiveness in the total European and world markets. This latter point applies particularly to the communications supplier industries. When captive markets in a country are lost because of deregulation of the carrier industry, it is essential for these suppliers to find new markets on a European or worldwide basis.

The regional telecommunications service operators in the U.S., resulting from the breakup of AT&T, have become important clients for European manufacturers. At the same time, these regional companies like NYNEX, Bell Atlantic, and others are attracting service business in Europe. But, in general, the European operating companies appear to be less open to American equipment manufacturers than vice versa. Because of high development costs, it is necessary for European manufacturers to reach total European markets and world markets in order to survive. Some companies in Europe; e.g., Plessey, Italtel, Alcatel, and Siemans, have formed alliances to share talent and development costs in some areas. They, at the same time, arrive at some standardization of products in preparation for the 1992 European Single Market.

The ten European manufacturers of digital exchanges provide more capacity than the European market can absorb. Therefore, it is necessary for them to sell to the American, Canadian, and Japanese markets, and they are successful. To improve their competitive situation, a variety of takeovers and alliances have been formed within Europe and trans-Atlantic. With the takeover of ITT subsidiaries in Europe, Alcatel is now the second largest telecommunications company in the world and has an immediate market share of the communications equipment market in many European countries. Links have been formed between AT&T and Philips, the Netherlands, in the form of a joint subsidiary called AT&T and Philips Telecommunications, and between AT&T and Olivetti of Italy. Philips and Siemens are working together on the production of microchips, the Megachip Project.

An important plan for Europe that will have a very great impact on all European industry, especially telecommunications, is the plan for an economically unified Europe. By 1992, the European Single Market will consist of 320 million consumers with wealth equal to that of the U.S. Frontiers are to be eliminated for the transfer of goods, personnel, and finance. There should then be a total European market for telecommunications equipment as contrasted with the present individual country markets. In preparation for this communications, service providers must standardize on matters like equipment acceptance tests and possibly tariffs for services. Manufacturers must ease the problem of adapting their products from country to country through standardizing to the extent possible. This is a major reason for the alliance between Plessey, Italtel, Alcatel, and Siemens in developing the next line of digital switching systems. The European Community (EC) is playing the major role in trying to achieve standardization of products, acceptance rules, and procedures.

Microelectronics

Microelectronics is the driving force for developments in both the computer and telecommunications industries. Contrasted with the U.S. and Japan in microelectronics, Europe's weakness has led to a concerted effort in Europe to catch up. Microelectronics in this context means mainly developing and manufacturing semiconductor components. This is a vital base technology which underpins a range of industries, especially computer and telecommunications industries.

Europe's trade deficit in electronic components is about $2.6 billion. The European production of electronic components was 14 percent of world production in 1978 and by 1987 was less than 9 percent.

The European market for semiconductors is substantial. In 1989, the 25 leading suppliers[1] (12 American, 9 European, 4 Japanese) had sales of $9.7 billion. These 25 companies accounted for about 97 percent of the total business. The European suppliers accounted for 36.7 percent of their own market, American suppliers accounted for 41.3 percent, and Japanese suppliers accounted for 19.7 percent.

In trying to increase Europe's share in the world market, the EC is taking the lead. Based on EC programs and national R&D program, steps are being taken to develop a strong technological base to create an internal market in information and telecommunications, and to develop a common policy of standardization in IT, telecommunications, and audio visual systems.

Philips and Siemens megaproject is directly aimed toward achieving European competitiveness in mass production microchips. The 4-megabit chip is now in pilot production. The individual circuits on the chip are 0.8-micron wide. The 4-megabit chip density was obtained by using a third dimension in the circuitry. So-called *ditches* one-micron wide and four-microns deep are made in the chip and memory circuits are put onto the walls of the ditches. Siemens and Philips have borne the DM 3.4-billion development cost. The respective companies have spent about DM 1.4 billion on developing the chip and DM 1.5 billion on constructing the production facilities. The respective governments have contributed about DM 500 million.

The Siemens-Philips combination has been joined by SGS-Thomson, the Italian-French semiconductor company in the Joint European Submicron Silicon Initiation (JESSI) program of EUREKA. Other European companies are expected to participate as well. This very large program, which will cost about 4 billion European currency units (ECU) for R&D and perhaps an equal amount to prepare for the production of its products, will be described more fully in a subsequent section.

In addition to mass-produced memory circuits, European companies are devoting considerable effort in developing and manufacturing application-specific integrated circuits (ASICS). The new European company--European Semiconductor Systems (ESS)--is concentrating on ASICS. Other established companies like Thomson, France, and Plessey, U.K., are emphasizing ASICS heavily.

[1]Source, Dataquest

European Strategic Programme for Research and Development in Information Technologies (ESPRIT)

The European Strategic Programme for Research and Development in Information Technologies (ESPRIT) is designed to promote European transnational cooperation in information technology (IT), provide the European IT industry with the technologies needed to meet the competitive requirements of the 1990s, and contribute to developing and implementing international standards.

The first phase of ESPRIT (1984-1988) was funded at 1.5 billion ECU; half was contributed by the EC and the participating organizations, respectively. Any established organization that is carrying out IT R&D within the EC is eligible to participate in ESPRIT. All ESPRIT projects must include at least two industrial partners from two different EC members.

The ESPRIT work program describes the strategy, objectives, and technical aspects of the work to be done. This work program is revised and published annually and is the basis of the call for project proposals. In the first phase of ESPRIT, the five research areas were (1) Advanced Microelectronics, (2) Software Technology, (3) Advanced Information Processing, (4) Office Systems, and (5) Computer-Integrated Manufacturing. As of the end of 1987, 143 out of the 227 ESPRIT I projects had produced industrially significant results (see Table 7).

Table 7. Industrially Significant ESPRIT I Results

Contributed directly to products or services currently available on the market (27)
Contributed directly to products or services being developed for the market but not yet commercially available (44)
Used outside the ESPRIT project, either within the company concerned or in another company (44)
Contributed to standardization, either adopted as an international standard or being elaborated by an international standards organization (28).

In December 1987, the Council of Ministers of Member States approved ESPRIT II. The 5-year phase has an overall budget of 3.2 billion ECU, half contributed by the participants and the EC, respectively.

In December 1987, the first ESPRIT II call for proposals was announced. The ESPRIT II program will continue to emphasize precompetitive collaboration research but will place more emphasis on the industrial nature of the program than did ESPRIT I (see Table 8).

Some prominent examples of successful projects are provided in the following paragraphs.

Table 8. ESPRIT II

ESPRIT II will
Provide a sustainable European capability in ASICS
Provide the technologies needed for the next generation of information processing systems
Enhance the capability of European industry to integrate it into complete application systems, in a broad range of differing environments.

The Transputer Project

The objective is to develop a high-performance multiprocessor computer with supporting software and a range of applications to demonstrate its performance. The basic design is a modular, hierarchical architecture based on reconfigurable nodes of transputers. Very large-scale integration (VLSI) switches, designed at Southampton University, U.K., under transputer control, determine the topology of the network within and between nodes. Reconfiguration

can be done during program execution under the control of the program. Hence, the configuration can be matched to the bandwidth requirements of the application.

A supernode consists of 16 worker transputers, each of which is a T800 which includes one 32-bit CPU, one 64-bit floating point unit, four standard transputer communication links, 4K bytes RAM, a memory interface and peripheral interface on a single chip using a 1.5-micron CMOS process.

The four links of each worker transputer are connected to a 72x72 VLSI switch which is controlled by a further transputer with its links connected to the switch. The 72x72 switch is implemented in two Nippon Electric Company integrated circuits, each functionally equivalent to a 72x36 crossbar switch. Each T800 has 256K bytes of external memory and the node has an additional transputer with 16M bytes of memory for storing and distributing data and code. A Winchester disk controlled by an M212 transputer can be included in the node. An internode switch is used to implement a three-stage network for reconfiguration between nodes. A control bus enables any transputer to communicate with the control transputer independently of the links. This is used for synchronizing and for debugging programs. The reconfigurable transputer processor supports static quasi-static and dynamic operation of the switched system.

The T800 is capable of sustained floating point performance more than one megaflop per second, and the estimated performance of a supernode with 16 worker transputers is more than 16 megaflops per second. Software is being developed for application in science and engineering, signal and image processing, image syntheses, computer-aided design (CAD) and computer-aided manufacturing (CAM). Resulting from the development in Project 1085, more than 200 parallel processors have been sold and are now being marketed in the U.K. by Parsys and in France by Telmat.

Portable Common Tool Environment Project

The Portable Common Tool Environment (PCTE) project has produced functional specifications of the PCTE interface, several implementations, and has provided a wide dissemination of the interfaces. In the PCTE approach, the center of the environment is a database, modeling the software activity it supports. The PCTE object management system accesses this database in response to requests made by any environment's component such as a file, a program, a report, or an abstract entry like a project or a team.

The PCTE manages all these objects in a uniform way. The PCTE provides a user interface that takes recent developments into account, including multi processing and the use of *windows*, enabling the user to interact with several tools concurrently. However, the system places primary emphasis on portability and on the provision of basic functions for developing new tools, while ensuring that existing tools; e.g., UNIX tools, were supported.

Two sample tools were developed to demonstrate using PCTE and to improve the overall quality: (1) a configuration management system emphasizes the facilities of object management systems, (2) the PCTE verification sites to assure the required compatibility of the PCTE with standards defined by the X/OPEN portability guide and the AT&T System V Interface definition.

Communications Network for Manufacturing Applications

The job of the Communications Network for Manufacturing Applications (CNMA) is to select, implement, validate, demonstrate, and promote communications standards for manufacturing within the framework of the International Standards Organization (ISO) reference model for OSI. The CNMA has concentrated on the upper layers of the OSI reference model especially on manufacturing message specification and file transfer, access, and management. This work complements work going on in the Manufacturing Automated Protocol (MAP) at General Motors and Technical and Office Protocols (TOP) at Boeing.

The CNMA profiles, documented in an implementation guide, are being implemented on numerical and process controllers and on minicomputers, on three types of local area networks (LAN) interconnected by routes: (1) IEEE 802.3 CSMA/CD Baseband, (2) IEEE 802.4 token bus broadband, and (3) IEEE 802.4 token bus carrier band.

In April 1987, a demonstration of the CNMA project was made at the Hannover Fair, FRG. The operation of a typical manufacturing cell involving controllers and computers from five vendors was demonstrated. The system is being demonstrated in production facilities at British Aerospace (BAe), BMW, and Aeritalia. The BAe pilot facility at Samlesbury is used to machine parts for the A320 Airbus. A precision boring facility is used to drill, bore, and ream a large array of parts for the A320 using leading edges. The BMW automobile plant at Regensburg uses CNMA to collect and compile maintenance and repair data from the factory floor to facilitate continuous operation of the production machinery. At Torino, Aeritalia's CNMA pilot facility concerns the production and control of cable forms destined for military aircraft.

Bipolar CMOS Project

This project combines bipolar integrated circuit (IC) processing and CMOS processing into a combined bipolar CMOS process taking advantage of the attributes of both. Bipolar has the advantage of high-gain and -speed processing while CMOS processing is characterized by low dissipation, ease of building complex circuits, and high process yield. A designer may then make large circuits with bipolar-like speeds and CMOS-like complexity and low dissipation.

Under this project, Philips and Siemens developed an IC technology combining bipolar and CMOS. In the first year, a technology called BICMOS O P using 2-μm lithography was used to begin testing electronic ideas and to calibrate the process simulation tools. In the second year, BICMOS 1 work began using a standard N well process, 1.5μm in Philips and 1.4μm at Siemens. Philips used an LDD structure in the NMOS and buried P and N layers while Siemens worked with Ta Si_2 gate and buried N layers. Despite these different approaches, it was possible to derive a common set of design nodes and a common set of test devices and circuits.

At Philips, the first results of BICMOS 1 P showed results that agreed fairly well with the theoretical prediction. At the end of the 2nd year, Siemens obtained very encouraging results. Consequently, by the end of the 3rd year, a 3-GHz bipolar transit frequency and a 500-MHz CMOS toggle frequency was obtained.

Human Factors for Usability Engineering

Project A of Human Factors in Information Technology (HUFIT) was designed to identify the critical steps in design that require human factors input and to incorporate human factor information into the IT product design process. The project has also developed tools that can deliver human factors information to designers in forms that they can readily use during the product design process, from conception to installation and use (see Table 9).

Table 9. HUFIT

Project A work activities will
Analyze the design and development processes undergone by IT products coming from large European manufacturers
Develop methods for describing task and user characteristics
Develop methods for implementing usability criteria and for evaluating models and prototypes during the design process
Gather and classify knowledge in computer human factors for consortium use and for designer dissemination
Develop human factors tools to assist in IT product design.

Project B provides theoretical and empirical knowledge about basic interaction modes for application in products with integrated human computer interfaces. The project has developed interfaces with improved usability and high efficiency. For future office tasks, more flexible interfaces will be needed that are adaptive or adaptable to user and task requirements. Project B investigated and developed interfaces integrating different interaction modes (see Table 10).

Table 10. HUFIT

Project B work activities will
Model human computer interactions
Operationalize the characteristics of different interaction techniques and define generic interaction techniques
Develop tools for defining and implementing integrated multimodel user interfaces as well as implement pilot schemes
Establish theory and practice in evaluation methods.

Parallel Reduction Machine Project

This project has taken what are considered to be good programing language styles and developed parallel architecture to support them. Two important breakthroughs have been made in the project: (1) natural parallel reduction model has been defined and (2) a distributed algorithm has been developed regarding counting garbage collection with low overhead.

Using experience gained from working with various parallel architectures for parallel graph reduction, especially COBWEB (a novel distributed memory architecture), a distributed memory architecture has been defined that supports the parallel reduction model. Emulation of this model could be helpful in understanding how a parallel reduction machine will work.

Optimization Steps in Silicon Compilation

A system has been developed for automatically generating circuits from algorithmic level descriptions. The algorithm is converted to a dataflow graph, which reflects the behavior of the algorithm and the constraints in the design. The dataflow graph is a basis for the structural synthesis. Dynamic programing is used in the structural synthesis. The resulting data path and controller are mapped onto transistor networks. The system can serve various layout styles.

CAD for VLSI Design

Advanced Integrated Circuits Design Aids was an R&D project for new VLSI design methods and corresponding CAD tools to master the growing complexity of VLSI circuits. Beginning in late 1985, a new generation of tools has been developed that will help the designer to apply his creativity for efficient and optimal design solutions. The special focus was on object-oriented data management of VLSI data; capture mechanisms of system specifications; logic synthesis; floor planning, advanced placement, and routing; a new generation of test aids, and other interface issues. Following the work plan, the team members have now prepared specifications for concepts and tools.

User Modeling in the Gradient Project

Several user modeling strategies are used in the gradient system to provide flexible support across different operators and to particular operators at various stages of expertise. The approach is to separate the role for operator modeling according to tasks within the gradient system. Distinction is made between the need for modeling operator's strategies in dialogue. A third facet of modeling is addressed in designer support tools which compliment the gradient system. The designer can employ an intelligent graphical editor which is complete with insight on the target operations in terms of display and domain-dependent graphical standards.

Large Area Complex Liquid Crystal Displays Address by Thin-Film Transistors

The next generation of office systems and portable computers will require a flat electronic display of page A4 size. Thin-film transistors addressing liquid crystal displays will allow an increase in display size and complexity from those required for word processor and graphic displays. The project has assessed the feasibility of making such a display and producing it at a competitive price. Excellent results have been obtained with both amorphous and polycrystalline silicon thin-film transistors. Both color and user interaction are incorporated into active matrix addressed displays.

Research in Advanced Communications for Europe (RACE)

Early plans for the Research in Advanced Communications for Europe (RACE)[1, 2] program were reported in *ESN* 39-3:122-123; a comprehensive description of the work of the definition phases carried out in 1986 was provided in ONRL Report 8-014-R; and the RACE Program in 1988 was described in ONREUR Report 9-7-C. This report will go into a little more depth in some areas of the work and will describe several projects started since the ONREUR Report 9-7-C was written. That report provided a brief description of Projects 1001 through 1048.

Nearly all of EC and European Free Trade Association (EFTA) telecommunications and telematics equipment manufacturers, as well as major users of telecommunications, are participating in the RACE program framework. The program is addressing the matter of providing Europe in a timely manner with advanced telecommunications services required for continued economic and political strength and for completing the European Single Market in 1992.

Joint teams of technical experts are collaborating in producing common functional specifications for Integrated Broadband Communications (IBC) and in developing the technologies required for applying advanced technologies in an economic fashion. Throughput, cost effectiveness, and technical performance are all important in arriving at the best solution.

Managing and transporting information throughout the world has a turnover of more than 500 billion ECU. The world market for telecommunications equipment alone is well over 80 billion ECU and the market for services is more than three times as large and is growing rapidly. By 2000, the EC will have invested an additional 500 billion ECU in telecommunications and the sector will account for about seven percent of Gross Domestic Product, compared with two percent in 1984. Inevitably, employment and the continued prosperity of Europe will be affected in a major way by the developments in telecommunications. In 2000, an estimated 60 million jobs in Europe will depend on the international competitiveness of Europe's information infrastructure and services.

The work in RACE addresses the technical and economic options for developing an advanced information infrastructure. However, strategic analyses of demand for powerful and cost-effective services determines the orientation of the technical work.

The first strategic audit of RACE was accomplished in 1988 by independent specialists who are familiar with key political and technical developments. The audit concentrated on global objectives and priorities, taking into account political, social, economical, technical, and industrial developments and the evolution of demand for advanced telecommunications. The conclusions were generally favorable and a second strategic audit was completed in the last quarter of 1989.

Within the EC, 11 telecommunications administrations, 89 universities and research establishments, and over 230 companies are now involved in RACE consortia. Organizations from 11 of the 12 EC countries are represented. Also, 32 organizations from Austria, Finland, Norway, Sweden, and Switzerland participate in 39 consortia. Although the RACE program is beginning a year later than planned, the excellent investigation during the 1986 feasibility study provides a plan of action supported by well-established facts about the current state of the art and reasoned conjectures about what might be achieved over a 5-year period.

RACE Projects Not Covered in ONREUR Report 9-7-C

Following are additional RACE projects, listed by project number and name:

1049 - Asynchronous Transfer Mode Concept. This project considers the specifications of header functions for Asynchronous Transfer Mode (ATM) cells and of the ATM layer protocol. Furthermore, this project will also address ATM-related signaling aspects.

1050 - IBC Application Analysis. This project deals with the analysis of applications to determine criteria to define the scope for IBC activities.

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[1]Research and Development in Advanced Communications Technologies in Europe, Directorate General XIII, Commission of the European Communities, March 1989.

[2]RACE: Consolidated Preliminary Report of the RDP Projects, Commission of the European Communities, Directorate General XIII, Telecommunications, Information Industry, and Innovation, June 1987.

1051 - Multigigabit Transmission in the IBCN Subscriber Loop. This is one of several customer access projects covering the topic of Customer Access Connection (CAC) using direct detection techniques. One project concentrates on a switch for interactive services and traffic engineering for the CAC, while the problems of passive optical components and the distribution switch are addressed by another project. Another project deals with very high bitrates (Project 1051, 5-10 Gbits/s). Although this project deals specifically with high bitrates for the CAC, it will also have relevance to long haul links. These projects emphasize reducing the cost of the customer access and the developing customer laboratory demonstration models.

1052 - Signal Processing for Optical and Cordless Transmission (SPOT).

1053 - TERRACE - Telecommunications Management Network (TMN). Evolution of Reference Configurations for RACE. This project is concerned with developing a set of reference configurations for the TMN, as part of the overall ICBN reference configuration. The study of an evolution scenario to a pan-European TMN is also one of the major objectives.

1054 - APPSN - Application Pilot for People with Special Needs. The aim is to support the elderly, deaf and hard-of-hearing, blind, and those with reduced mobility. The support services will enable service providers to be in immediate contact with the home-based person using a videotelephone. The project will provide for several service centers, each capable of supporting up to 100 special video terminals, on an analogue broadband, or digital 2 Mbits/s, or 64 Kbits/s, network of star topology.

1055 - MERCHANT - Methods in Electronic Retail Cash Handling using Advanced Network Technologies. The goal is to progress toward an advanced European electronic retail payment system with plastic cards that will consider IBC. This will be achieved by connecting nonconnected networks, by developing user interfaces with image, voice and data, and finally, by ensuring that security aspects are considered.

1056 - BIPED. This project contributes to the area of IBC customer systems and integration in such a way that it allows an early integration of terminals, customer premises networks (CPN), CAC, and local exchange. The scope is slightly broader than that of Project 1056, since many terminal projects are involved in Project 1081. However, both projects are closely related and even physical integration is foreseen between these two projects. They also contribute to verification.

1057 - AQUA - Advanced Quantum Well Lasers for Multigigabit Transmission Systems. This project intends to achieve high-modulation bandwidth, together with high power output and efficiency. Good temperature stability and a thorough understanding of carrier transport and relaxation mechanisms are also important objectives.

1058 - RESAM - Remote Expert Support for Aircraft Maintenance. The objective is to develop and evaluate the usability of an information system for aircraft maintenance to improve security for the users and reduce costly immobilization time for the aircraft on the ground. This will be a conferencing system with voice, text, graphics data, image, and video communication. Databases from the company and the manufacturer will be included, also authentication and encryption of information.

1059 - DIVIDEND. This consists mainly of videophone service enabling eye-to-eye contact between dealers in the financial dealing sector, using a broadband communications network.

1060 - DIDAMES - Distributed Industrial Design and Manufacturing of Electronic Subassemblies (RPA). Application of local and wide-area broadband networks within a distributed industrial design and manufacturing system for electronic subassemblies (multilayer printed circuitboards). This will consider the sharing of CAD/CAM techniques between design and manufacturing locations, supported by a voice- and video-based teleconferencing system, and will demonstrate the usefulness of international data interchange standards.

1061 - DIMPE - Distributed Integrated Multimedia Publishing Environment. This project is attempting to create an environment enabling a wide range of commercially viable publishing services to be provided over the IBC. The project places great emphasis on obtaining a clear understanding of user requirements. The project will use existing technologies; e.g., peripheral publishing equipment, and the broadband network infrastructure. The project will also focus on and promote all aspects of standardization in this application area.

1062 - MARIN-ABC. The aim is to demonstrate using broadband/narrowband communications in the maritime industry, and more precisely, to help solve shipboard nonroutine maintenance and repair problems with the

assistance of shore-based experts. This will involve using data and voice, together with still- and moving-picture transmission.

1063 - Mobile Applications Pilot Schemes. The project consists of four applications which are intended to demonstrate the need for mobile communications: (1) broadcaster's production communications/major event coverage; (2) courier services; (3) public utilities, operation, and maintenance; and (4) rail transport.

1064 - Monolithic Integrated Optics for Customer Access Applications (MIOCA).

1065 - ISSUE - IBCN Systems and Services Usability Engineering. This project will investigate experimentally the important usability issues of videocommunication and multimedia retrieval services, using emulation techniques. The project will develop through a multidisciplinary approach. The aims of the project are to identify the main factors governing services' acceptability to users and to provide inputs to the RACE usability database and application pilots.

1066 - IPSNI - Integration of People and Special Needs by IBC. This project will include study of the functional requirements for enabling visually and motor/speech handicapped people to use IBC terminals and services.

1067 - GUIDANCE - Usability Design Information Support for the Integration of IBC Services. The purpose is to cover the issues of integrated dialogue and retrieval services. The project will use the multimedia terminal from Project 1038 as its vehicle for experimentation.

1068 - ROSA - RACE Open Services Architecture. This area, which is particularly relevant to telecommunication software, includes the technique to provide and integrate services. Service provision is the fast-growing branch of telecommunications. Probably the major obstacle in satisfying the needs of potential users is the difficulty to produce the corresponding software, because the current generation of telecommunication systems tend to be intractable and unwieldy in the face of rapidly changing requirements. This project will develop and define an open architecture for distributed on-line telecommunications systems specially designed to considerably reduce the cost and time to introduce future facilities, features, and services.

1069 - EPLOT - Enhanced Performance Lasers for Optical Transmitters. This project is directed towards high power output and power handling for optical amplifiers. Narrow line-widths for use in Coherent Multi-Channel and Wave Division Multiplexing applications is a prime target, as is low reflection sensitivity.

1070 - Testing Pay-Per-View in Europe. In this project, pay-per-view TV will be tested in these locations: Biarritz, France; Limburg, Holland; and Berlin. An appropriate man-machine interface, with as many common elements as possible, will be developed to ensure comparability of the results from these tests. Specialized software for traffic modeling and evaluation tools will also be developed to assist in determining strategies for the introduction of pay-per-view and the transition to IBC.

1071 - IBC Application Analysis (Phase 2). This project deals with the analysis of applications, to provide a basis to develop entry strategies and pilots for IBC, and to enable IBC services to achieve maximum momentum, using empirical and robust data.

1072 - ITACA - IBCN Testing Architecture for Conformance Assessment. Project ITACA expects to identify the methodologies, procedures, and tools needed to define an IBCN conformance testing system able to handle the high data rates of IBCN. Testing tools and equipment will not be produced, but the relevant requirements will be specified.

1073 - GEOTEL. This project will create a library service for the petroleum and chemicals industries. Two main servers, located in London and Paris, will use optical disk data storage and workstations spread throughout Europe. The data bank will include patents, CAD/CAM drawings, and seismic surveys.

1074 - ECHO - Electronic Case Handling in Offices. This application pilot is concerned with installing an electronic case-handling system within an existing department of an insurance company to automate a currently paper-based process. The distributed system of workstations and servers on a local area network (LAN) at one location will use a public broadband network to communicate with other locations. The workstations will have high-resolution screens with advanced graphical user interfaces and the servers will be dedicated to the storage of databases, images, and voice information on both magnetic and optical media.

1075 - TELEPUBLISHING. This project is to bring the European printing and publishing industry and users of their equipment up to the current state of the art in computer, software, and communication technology. This application is designed to demonstrate a future working scenario in a broadband environment, to allow easy and time-saving interaction between distributed locations of the printing and publishing industry. The application should realize all functions from design, layout, text, and image producing down to printing and producing.

These domains are targeted: electronic newspaper editing, school textbooks, and magazine printing, in which there is currently a high degree of incompatibility of the equipment and transmission protocols. The project will thus focus on standardization aspects for the edition of documents, document exchange, and the open interconnection and exchange of information between heterogeneous systems.

1076 - REMUS - Reference Models for Usability Specifications. The REMUS objective is to establish a database of agreed upon usability design targets for the relevant user/task/tool environment combinations in the IBC applications. The database should help the IBC system, services, and terminal designers to develop man/machine interfaces that are consistent across a wide range of applications.

1077 - Usage Reference Model for IBC. This project will provide Usage Reference Models for the different types of usage design issue. Three areas are dealt with: establishing the Conceptual Framework; collecting and synthesizing usage data with Usage-FRM mappings & Usage-RC mappings; and Usage Reference Data output to RACE designers and standards/external bodies.

1078 - European Museums Network. The purpose is to demonstrate the usefulness of broadband communication in the cultural field and use the so-called associative approach to give a visitor to one museum, among 15 in Europe, access to information in the archives of the others. Thus, the visitor can obtain details or explanations of an artwork; e.g., a painting, object, or sculpture, that is not physically available at the museum being visited. The network will use multimedia workstations and mix still images, video images, sound, music, and text.

1079 - CAR - CAD/CAM for the Automotive Industry in RACE. The objective is to integrate the design team, the manufacturing plants, and parts suppliers into one distributed entity. CAR aims to improve the efficiency of the European automotive industry by accelerating design to production timescales and the modification processes. Additionally, it will provide a better coverage of information for all involved including car dealers. Also, it will investigate using video/voice communication, in addition to high-speed data communications to strengthen human-to-human relationships in a high-technology environment.

1080 - HDTV Experimental Usage. Following the demonstration of the EUREKA 95 equipment at IBC '88 Brighton, U.K., the purpose of this project is to acquire practical experience with this evolutionary, compatible HDTV system. Also, it will provide facilities for using the European HDTV approach experimentally, which will demonstrate the complete range of HDTV production tools, including emission, and reception equipment, by using them to cover major events in and outside Europe.

1081 - BUNI - Broadband User Network Interface. Both Projects 1081 and 1056 contribute to IBC Customer Systems and Integration in such a way that they allow an early integration of terminals, CPNs, CAC, and local exchange. Since many terminal projects are involved in Project 1081, its scope is slightly broader than Project 1056. Also, the two projects will measure quality and service to verify whether service requirements can be met. These measurements will be supported by Project 1083 which will provide a traffic analyzer and generator.

1082 - QOSMIC - QOS Verification and Tools for Integrated Communication. Project 1082's objectives are:

- To define IBC quality-of-service requirements by analyzing existing networks, analyzing QOS requirements of IBC services, and evaluating QOS verification techniques
- To define QOS verification methodology and mapping QOS to network performance
- To document QOSMIC assumptions and requirements.

1083 - PARASOL - ATM Specific Measurement Equipment. This project will study aspects of measuring and verifying technologies required to support introducing ATM technology for Integrated Broadband Communication Networks (IBCN).

1084 - MIME - Development of Emulators and Simulators. This project will handle the TMN requirements for emulators and simulators. Identifying those other areas of the IBC in which the application of emulation and simulation will have an impact and produce suitable emulation/simulation systems.

1086 - TELEMED. The main objective is to demonstrate IBC's potential for medical record transmission, management, and control allowing clinical and research staff to work together on diagnosis and therapy methods using multimedia workstations.

1087 - PROVE - Provision of Verification. The main objectives of this project are to:

- Recommend standardizing methods and procedures to verify IBC
- Recommend reducing the need for and simplify the interoperability testing
- Define testability and maintainability concepts and propose a strategy to introduce the concepts into the design phase
- Recommend a methodology for computer-aided generation of test cases
- Collect all information necessary to establish a common verification testing and maintaining concept
- Recommend access for verification of IBC, supported by test reference configurations
- Standardize methods and procedures for verification by supporting the 1045 Consortium activities with technical expertise
- Establish feasibility for the following verification tools: traffic load generator, interfaces to ATM/Hybrid system access, and signaling control unit
- Develop prototypes as recommended by the October '89 Audit Panel.

1088 - TUDOR - Usability Issues for People with Special Needs. The main objective is to consider special needs within the general population; e.g., elderly and handicapped, in IBC design.

TV and HDTV in the RACE Program Context

The RACE program is concentrating on IBC where telecommunications services such as voice and data are integrated with visual services such as TV distribution to merge the two main streams of communication. The most stringent requirements for bandwidth are those arising from the visual services. Even though RACE was conceived by telecommunications specialists, the importance of TV was never disregarded and the RACE workplan provided for a fair amount of activity.

The response to the first call for proposals established a credible framework for TV-related activities. Embedding the EUREKA 95 Project into this framework considerably enhances RACE's visibility in the TV context. The activities related to TV/HDTV in RACE cover the chain from the studio to the TV user. The work currently under contract in RACE corresponds to a total effort of about 300 million ECU (see Table 11).

Table 11. RACE-Related Projects

Studio. Project 1036 deals with Wavelength and Time Division Multiplexed Broadband Customer Premises Network (TV/Studio).

Switching. Switching projects address all switching services, however the most stringent requirements are posed by video switching:

1012: BLNT - Broadband Local Network Technology
1014: ATMOSPHERIC
1022: Technology for ATD
1013: HDTV Switching

Video Coding

1018: HIVITS - High Quality Videotelephone and High Definition Television System
1041: FUNCODE Functional Specification of Codes

Transmission

1051: Multigigabit Transmission (10 Gbit/s)
1030: Access
1010: Subscriber CMC System

Terminals

1001: Digital Video Tape Recording Terminal for HDTV

Demonstrators

1080: HDTV Experimental Usage (EUREKA 95)

Mobile Communications in the Context of the RACE Program

The concept of IBC, as understood by the RACE Program, requires satellite and mobile communications, as well as the terrestrial fixed network aspects, to be considered. The mobile services are expanding rapidly as the cost of mobile terminals drops, and before the end of the century, a low-cost pocket telephone will be possible and desirable. Also, existing mobile communications are provided by overlay networks linked to the fixed networks at only a few points.

In the context of IBC, mobile communications are considered as an integral part of IBC, and several tasks in this field appear in the RACE workplan. Project 1043, in which many major industries and primary telecommunications operators in the area participate, was incorporated in the RACE Program following the first call for proposals. The cooperation between the partners of the two sectors will ensure its technical viability, as well as a high degree of acceptance among the telecommunications operators.

Project 1043 is paying special attention to the impact that mobile communications have on the fixed network. Compared with the fixed network, public mobile communications is in its infancy, but evolving very quickly, driven by commercial pressures. Ideally, any IBC service available on the fixed network should also be available to the mobile user. However, frequency spectrum and economic constraints limit the practical possibilities.

The second call for proposals identified activities on verification to permit a cost-effective integration of mobile communications into IBC while providing the required quality of service level. Project 1043 is undertaking all activities in mobile communications. Project 1063 also addresses mobile aspects. Four pilot schemes are thereby established that will demonstrate the need for and the utility of various mobile aspects of IBC. Project 1043 covers two main classes of mobile service:

1. Universal Mobile Telecommunications System (UMTS) to provide speech and low-to-medium rate data service; this is to achieve virtually complete geographical coverage

2. Microwave Broadband to provide very-high bit-rate connections to mobile units.

Such systems cannot, in the foreseeable future, provide complete geographical coverage but will be important for certain specified applications.

The UMTS goal is a standard flexible air interface for all classes of service; e.g., cordless telephony, cordless PABX, cellular radio. The UMTS concept is an approach within RACE that is expected to evolve during the course of the program (see Table 12).

Table 12. UMTS Key Elements

A common standard for public cellular systems and private cordless telephones with full interworking
Very low-cost personal terminals; i.e., a mass-market pocket telephone
An infrastructure comprising a mixture of public and private cells connected to the IBCN to allow growth constrained only by economics
High bit-rate radio channels designed to carry a wide-range of data services including video and graphics, short messages, and large data files.

The core tasks of the project are: fixed network mobile functions, mobile system and services, radio bearer, cellular coverage, channel management, signal processing, technology, mobile broadband services, and verification models for different networks.

The RACE Mobile Application Pilot Schemes (Project 1063) has four pilot schemes designed on the principle of a scale model in which a small group of users will receive a service using, as far as possible, existing technology. The pilots are concerned with: broadcasters' production communications/event coverage, courier services, public utilities, operation and maintenance, and rail transport. The projects should generate justification for allocating additional frequencies in the radio spectrum for mobile communications.

European Research Coordination Agency (EUREKA)

Background

The European Research Coordination Agency (EUREKA) program resulted from a proposal made in 1985 by French President Mitterand (see *ESN* 40-4:141-142, *ESN* 41-1:12-15, and ONRL Report 8-009-R). Since its launch during a first ministerial meeting in Paris in July 1985, six further ministerial meetings have been held at which projects were approved. At Hannover, FRG, in November 1985, the first 10 projects were approved. A further 60 projects were adopted during the third ministerial meeting held in London on June 30, 1986; at the fourth conference in Stockholm in December 1986, 37 more projects were approved; in the Madrid meeting of September 15, 1987, the total was brought to 165, with the adoption of 58 further projects; and in the Copenhagen meeting of June 15-16, 1988, the total was brought to 214; and in the Vienna meeting of 1989, the total became 291. The dominant fields of technology in the adopted projects are information systems, biotechnology, and production technology. The cost of the development effort in the 291 projects is about 7 billion ECU over the lifetime of the projects.

Currently, there are 20 EUREKA members--19 countries and the EC. The countries are Austria, Belgium, Denmark, Finland, France, the FRG, Greece, Iceland, Ireland, Italy, Luxembourg, the Netherlands, Norway, Portugal, Spain, Sweden, Switzerland, Turkey, and the U.K.

Purpose

The EUREKA program is intended to serve as a Europe-wide organization to encourage collaboration on the part of its members on advanced technology projects. Approval is normally given to serious proposals involving cross-border collaboration on civilian projects between firms and research institutes from different EUREKA members, regardless of size or structure. No centralized source of funds is available. Projects are funded by participating firms and institutes and their respective governments in some cases. The expectation is that these projects will strengthen the competitive position of European products, processes, and services throughout Europe and overseas in both public and private markets.

There are no predetermined technology areas. Companies, universities, and research institutes decide to collaborate in their own areas of interest based on the advantages they see in their collaboration. Individual firms or institutes determine the topics on which they wish to collaborate, then they seek partners who are willing and able to contribute to the work. Associations made in ESPRIT, RACE, or BRITE probably play a part in determining partnerships. The proposed partners, with the assistance of their national government officials, are responsible for bringing their ideas and concepts to the attention of the EUREKA ministers for approval. Governments or the EC may choose to propose and promote a project whenever its size, complexity, or objectives are of sufficient national or international interest. EUREKA is, in effect, a clearinghouse in the search for industrial, scientific, and financial partners throughout Europe.

Operations

The EUREKA Secretariat, located in Brussels, circulates project proposals and expressions of interest to the national authorities, when they are received, and the national authorities pass on the information to the other firms or organizations that may be interested. Constraints and obligations are kept as simple as possible so that, for example, additional partners may enter a project once a partnership has been formed, with agreement of the existing partners. Obligations concerning disclosure of results derived from EUREKA projects may be tailored to the particular needs of participants.

Through EUREKA, companies may request supportive measures from their own national governments or from the EC to help with cross-border cooperation in R&D. These measures necessarily relate to areas in which national governments and the EC may directly or indirectly influence the system for cooperation. Through these measures, EUREKA should lead to a speedup of ongoing efforts to: eliminate existing technical obstacles to trade by the mutual recognition of inspection procedures, elaborate joint industrial standards at an early stage, and expand the public procurement system.

Participants in EUREKA are expected to find the required funds themselves, either internally or by seeking financial partners, using private financial sources such as the capital market or loans or any public funds that they may receive

from their national governments or the EC. Within the initiative, contacts with groups of banks and venture capital associations have been established with the aim of mobilizing more private sector funds for high-technology projects (see Table 13).

Table 13. EUREKA Project Breakdown

Information technology	25.0 percent
Robots and manufacturing	17.5 percent
Biotechnology	13.0 percent
New materials	12.0 percent
Environment	8.3 percent
Telecommunications	7.4 percent
Transport	7.4 percent
Energy	5.6 percent
Lasers	3.8 percent

The procedure for a proposal is for each partner or partners of each involved country to submit the proposal to the country's national coordinator. The concerned national authorities will examine the proposal, approve if appropriate, and transmit to the EUREKA Secretariat. The EUREKA Secretariat will check the proposal, register it in the EUREKA database, and circulate it among members and the EC. The proposal is then submitted to the next ministerial conference for review and approval. Two of the most prominent EUREKA projects are its HDTV project--EUREKA 95--and its JESSI project--EUREKA 127--both of which are briefly described in the following paragraphs.

Compatible High-Definition Television System

The objective of this project is to develop a 50-Hz-based HDTV system along an evolutionary development from the Multiple Analog Component (MAC)-Packet concept, retaining compatibility with MAC transmitters and receivers. The emphasis in Europe is on the future possibility of HDTV delivery on new services. Any new service such as Direct Broadcast Service (DBS) or Microwave Video Distribution (MVDS), which uses a different frequency band from current transmissions and/or a different modulation scheme, will inevitably mean that the next consumer will need a converter to interface with his existing TV receiver.

Such new services are incompatible. Whether the new service uses conventional color coding Phase Alternating Line (PAL), Sequential Couleur A Memoire (SECAM), or a new system is then a secondary issue. The MAC concept has emerged as a new standard in this context because it offers sufficient benefit to the service provider and consumer alike that it warrants the marginally increased decoder cost compared with PAL/SECAM. The MAC concept allows for introducing HDTV in a compatible, evolutionary way. The U.K. DBS service should introduce HDTV onto any or all of its program channels at any time by using HD-MAC coding techniques. The HD-MAC was conceived to be a compatible signal with MAC. In fact, the European MAC system can be considered a form of Extended Definition TV (EDTV) since it is based on a 625-line/50Hz accommodated in the units required to receive the MAC transmissions. Also, MAC permits widescreen pictures to be transmitted. The European 1250-line/50Hz EUREKA Project 95 system has been demonstrated.

Joint European Submicron Silicon Initiative (JESSI)

The Joint European Submicron Silicon Initiative (JESSI) project began as a 1-year feasibility study under EUREKA and was approved in December 1986. Carried out in 1987, the study concluded that a thriving microelectronics industry adds new values to a country's economy, which are many times more than its intrinsic contribution. The study also concluded that in many areas of IC production and IC applications, the U.S. and Japan ranked ahead of Europe.

As a result of the study, the national consortia for submicron technology in France, the Netherlands, and the FRG proposed the JESSI project as a Europe-wide EUREKA program. The objective is to have, in Europe, a resourceful microelectronics industry with a production volume reaching at least the size of the European market for microelectronics by 2000.

A definition phase for JESSI as a Europe-wide program began in January 1988 and resulted in a confidential document of some 800 pages. An acceptance phase extended from January to June 1989. The recommended funding level for R&D is 3.8 billion ECUs over an 8-year period; it has been estimated that an equal amount will be required to prepare and activate facilities and equipment needed for manufacture. The major participants originally were Siemens and Philips, because of their ongoing work on the Mega project, which has produced 4 megabit dynamic random access memory (DRAMS) for the market. SGS-Thomson is now also a major participant and others are expected to join. On March 5, 1990, it was announced that IBM would join the JESSI program.

The program objectives will include developing the technology to produce memories and logic using 0.3-micron feature size by 1995. The production 4-megabit DRAMS use 0.7-micron circuits, the future 16-megabit DRAMS are expected to use 0.5-micron circuits, and the 64-megabit DRAMS will use 0.3-micron circuits in 1995.

Basic Research in Industrial Technologies in Europe/ European Research in Advanced Materials (BRITE/EURAM)

Introduction

The Basic Research in Industrial Technologies in Europe/European Research in Advanced Materials (BRITE/EURAM) programs combines the BRITE and EURAM programs. The first research under the BRITE program started in early 1986 and under EURAM in late 1987. The BRITE evaluation panel judged that 80 percent of the projects were progressing well. The program had helped to consolidate industrial transborder alliances and to create new ones; it had benefitted small- and medium-sized companies through involvement in research and the resulting market opportunities. Smaller and underdeveloped states had participated fully in the BRITE program. Finally, a substantial number of important results are appearing that depended on transborder collaborative research.

The advance notice of the first call for proposals for BRITE/EURAM was published in July 1988, and the first call for proposals was made in December 1988. The deadline for proposal submission was March 15, 1989, and the contracts started in December, 1989.

The Technical Content of the BRITE/EURAM Program

With a budget of 439.5 million ECU for 1989-1992, the program will concentrate on the R&D most likely to meet goals critical to competitiveness of the EC's manufacturing industry. The technology areas were selected after extended

consultation. This involved inputs from a postal survey of 1,000 companies, from individuals and professional and trade associations, and from industrial technologies and advanced materials working groups of the Industrial Research and Development Agency Committee. These four technical areas of the new program are described in the following paragraphs:

1. Advanced Materials Technologies

This area will concentrate on developing, processing, and applying improved or new materials, and material processing. The work will cover materials and composites based on metals, polymers, and nonmetallic materials, and will cover materials for a range of specialized applications. However, developments of materials already covered by ESPRIT are dealing with magnetic, magneto-optical, optical thin films for sensors, recording media and heads, optical layers and specific materials for optoelectronics, ceramics, and polymers for integrated circuit packaging and substrates, and superconducting thin films for low-current applications and devices. These will be excluded from the BRITE/EURAM Program in cases where there is an overlap.

- Metallic Materials and Matrix Composites. A particular focus of this class of materials is in those industries where improved materials can be exploited by designers to reduce operating and maintaining costs, including savings in energy necessary for success in the market (see Table 14).

Table 14. Metallic Materials and Matrix Composites Goals

Extended working life of components
Higher operating temperatures for increased thermal efficiency
Better and more effective material processing techniques.

- Materials for Magnetic, Optical, Electrical, and Superconducting Applications. For example, polymer-bonded anisotropic permanent magnets or massive segments of metallic glass for applications such as electric motors, security systems, ore separation, medical equipment, and magnetic levitation for transportation vehicles are examples of uses. Optical materials are important for optical communication such as laser beam delivery systems. Among materials for electrical applications are those for electrochemical devices. High-temperature superconductivity materials may have use in components for reduced energy consumption. The goal will be improved materials and materials processing for the above.
- High-Temperature Nonmetallic Materials Goals (see Table 15)

Table 15. High-Temperature Nonmetallic Materials Goals

Design methods for products based on ceramics, glass, and amorphous material
Improve monolithic and ceramic composites, and metal/ceramic interfaces for industrial applications
Improve processing techniques and quality control strategies.

- Polymers and Organic Matrix Components Goals (see Table 16)

Table 16. Polymers and Organic Matrix Components Goals

Develop polymers for specific applications
Achieve more cost-effective process techniques for parts made from polymer and polymer-matrix composites
Design rules for specifying and manufacturing engineering polymers and composites
Develop new polymers with improved recycling attributes
Improve product assurance techniques.

- Materials for Specialized Applications. This sector will deal with improved materials for the packaging industry, biomaterials, and more advanced materials for the building and civil engineering industry. The goal will be improved materials and their processing for these specialized applications.

2. Design Methodology and Assurance of Products and Processes

Developing techniques to improve product quality and the reliability and maintainability of structures, and manufacturing systems by clarification of the design aims for both product and process, and by refinement of the criteria against which the attributes are measured area objectives. Exploitation of materials for sensors and the reduction in the whole life costs of sensors are included in this program.

- Quality, Reliability, and Maintainability in Industry Goals (see Table 17)

Table 17. Quality, Reliability, and Maintainability in Industry Goals

Improve performance measurement for manufacturing operations in a wide variety of industries
Improve and make more predictable physical and environmental behavior of products
Improve quality control strategies
Design rules for reliability and maintainability of components, structures, and systems, including machinery operating under varying conditions.

- Process and Product Assurance Goals (see Table 18)

Table 18. Process and Product Assurance Goals

Reduce whole-life costs of sensor systems for process control
Exploit materials properties for application in sensors
Use advanced measurement techniques for more cost-effective examination of topology
Improve energy control for industrial application
Improve nondestructive testing methods for product assurance.

3. Application of Manufacturing Technologies

The task is to identify and address the needs of the manufacturing industry, particularly the less advanced sectors, many of which are made up of small- and medium-size companies. Modeling of physical processes will be a valuable instrument for progress. The use of flexible materials will be addressed. The work will mainly emphasize product and process development transferring and adapting technology already used in other sectors. This should complement work in ESPRIT where IT systems for advanced manufacturing and CAM are being developed.

- Advanced Manufacturing Practices Goals (see Table 19)

Table 19. Advanced Manufacturing Practices Goals

Identify means for improving manufacturing practices in specific sectors
Transfer and adapt technology already used in other sectors.

- Manufacturing Processes for Flexibility Materials Goals (see Table 20)

Table 20. Manufacturing Processes for Flexible Materials Goals

Increase process flexibility
Reduce materials waste
Improve process and product quality.

4. Technologies for Manufacturing Processes

- Surface Techniques. With a better understanding of how surfaces systems behave, it should be possible to model systems to optimize selection. With some exceptions, such as in parts of the process industry, it is unlikely that existing knowledge is sufficiently complete to support using expert systems to justify their development.

  This is an area where collaboration is needed to bring complementary expertise together and ensure that equipment suppliers and users are able to integrate the different technologies into cost-effective applications using advanced information-handling technologies (see Table 21).

Table 21. Surface Techniques Goals

Cost-effective surface treatments for industrial applications
Quality assurance techniques and process control process treatment.

- Shaping, Assembling, and Joining Goals (see Table 22)

Table 22. Shaping, Assembling, and Joining Goals

Improve methods for shaping and assembling
Improve joining techniques to improve reliability and reduce defects
Design methods for testing and bonding welded joints to improve reliability of results and service predictability
Design method for joining
Understand beam/workpiece interactions for industrial power beam processes.

- Chemical Processes Goals (see Table 23)

Table 23. Chemical Processes Goals

Improve predictability and yield in chemical processes
Obtain membrane materials with improved characteristics
Improve performance of membrane processes
Obtain new systems for separation in hostile environments.

- Particle and Powder Processes Goals (see Table 24)

Table 24. Particle and Powder Processes Goals

Improve techniques for particle production to optimize product shape, structure, and stability
Obtain cost-effective techniques for particle categorization and process performance
Obtain better approaches to handling and separating
Obtain cost-effective methods for small lots of high-quality powder.

- Implementing BRITE/EURAM in a Global R&D Context

Industry has confirmed the requirement for a better awareness of emerging technological development as an important element of the technology strategy of large and small industrial companies. For reinforcing the market pull of the BRITE/EURAM program, this awareness is needed. The EC will take further initiatives, including workshops, in consultation with other agencies. The aim is to bring together the global science and technology (S&T) trends with the planning needs of individual companies realizing that this cannot be limited to a single sector but must also involve related sectors in which are major customers and existing or potential suppliers of materials, equipment, and expertise.

The program will be open to enterprises from all sectors of industry and research organizations, including universities within the EC and EFTA countries. Projects involving partners from EFTA countries will be welcomed where their participation can contribute to the competitiveness of the manufacturing industry as a whole. The projects must fulfill the normal eligibility criteria with the EFTA partner being additional to the requirement that there be at least two legally independent industrial enterprises from at least two different EC members. There will be no financial contribution from the EC toward the participation costs of partners from EFTA countries who will be required to contribute to the program overhead.

Within the program, there will be four separate forms of support. The industrial applied research will be the principal action with over 90 percent of the budget. There will also be focused fundamental research with up to seven percent of the budget. Feasibility awards for small- and medium-sized enterprises will get about 0.5 percent of the budget and coordinated activities will receive about 1.5 percent. Past experience in BRITE/EURAM indicates the following breakdown for expenditure by category (see Table 25).

Table 25. BRITE and EURAM Expenditures

	Percent
Advanced materials applications	30.0
Design and assurance of products	21.0
Manufacturing systems	21.0
Technologies for manufacturing processes	21.0
Administration	2.5
Personnel	4.5
	100.0

Chapter II
Significant National Programs

The United Kingdom

The U.K. has been the European leader in privatization and liberalization in the telecommunications industry. Until 1979, British Telecom was part of the government-owned Post Office monopoly. In 1984, British Telecom (BT) was privatized through sale of 51 percent of BT shares to the public. At the same time, BT and Mercury provided basic telecommunications service and Oftel monitored to oversee the competition between the two service providers.

Mercury has invested £350 million in its own networks. There are also two competing networks for mobile telephone services--Orbitel and Cellnet--with over 230,000 users between them. The VAN services now exceed £150 million and customers can choose among 450 telephone suppliers. Mercury is also authorized to supply callbox service in competition with BT; however, BT continues to invest £2 billion annually in infrastructure.

The U.K. also established several government-sponsored national programs for R&D ahead of similar EC programs. The Alvey program is notable in the IT industry; the 5-year phase ended in April 1988. These national programs are discussed in the following paragraphs:

U.K. National Programs

JOERS

The JOERS program began in December 1982, with a £25-million budget that was initially allocated to 21 collaborative projects involving 15 companies and 23 higher education institutions. Because of the high demand for JOERS funds, a second £11.25 million was committed in March 1986, allowing for 10 additional programs.

The JOERS program mission is to perform the research needed in optoelectronics for products in the market. This involved invention and exploitation of the results. Because JOERS was the first major collaboration in the U.K. between companies and educational institutions, it was a trailblazer for other programs, including the Alvey program.

The program appears to have succeeded in its aims: increased collaboration between industry and educational institutions leading to a better understanding and appreciation of each other's working methods and needs; maintaining research in optoelectronics where it might not otherwise have happened; and success in the research which should lead to exploitation by companies.

LINK

The purpose of LINK is to accelerate the commercial use of government-funded research. The LINK initiative will stimulate collaboration between industrial and science partners on projects in key areas of S&T. This should facilitate exploiting new processes, and developing and marketing new products and services by industry.

The first five programs under LINK, at a cost of £83 million, were announced in February 1988; half of the cost will be provided by the government. The LINK program expenditure over the next 5 years is expected to reach at least £420 million (see Table 26).

Table 26. LINK Programs

Molecular Electronics. Supported jointly by SERC, DTI, and industry; cost - £20 million. Emphasis on molecular materials with potential use for applications in electronics. Interested organizations: Thorn EMI, Pilkington, BDH Chemicals, Mullard and British Aerospace, Hull and Durham Universities, and Cranfield Institute of Technology.

Advanced Semiconductor Materials. Supported by DTI, SERC, and industry to improve the performance of microelectronic and optoelectronic devices by making available better materials and fabrication methods; cost - £24 million. Concentration on material studies mainly on multilayer structures, including silicon. Interested organizations: BT, Philips, Plessey, STC, MCP Electronic Materials, Epichem; Glasgow, Sheffield, Nottingham, and Liverpool Universities.

Industrial Measurement Systems. Supported by SERC, DTI, and industry, concentrating on developing advanced, integrated instrumenting and measuring systems for improving quality and efficiency in the manufacturing and processing industries; cost - £22 million. Over 50 projects involving a wide range of universities and companies have been submitted in outline.

Eukaryotic Genetic Engineering. Supported by DTI, SERC, and industry; cost - £4.7 million. Designed to increase the understanding of molecular genetics, particularly of yeasts, fungi, plants, and animals, including plant and mammalian cells in culture. Interested organizations: Glaxo, Whitbread, Dalgetty, British Biotechnology; Oxford and Leicester Universities.

Nanotechnology. Supported by DTI and industry; cost - £12 million. Will be working with new technologies for machining, positioning, controling and measuring to an accuracy of one nanometer (10^{-9} meters). Interested organizations: Ferranti-Astron, STL, Oxford Applied Research; Warwick, Reading, and Aberdeen Universities.

Alvey Program

Alvey was a 5-year IT research program that ran from May 1983 to May 1988 and involved 200 industrial and 117 academic-only projects. The program was funded at £350 million, of which £200 million and £150 million came from the government and participating companies, respectively. The five key sectors of research were: VLSI, Software Engineering, Intelligent Knowledge-Based Systems, Systems Architecture, and Man/Machine Interface.

An outstanding feature of the program has been the readiness with which industrialists and academics have formed close and harmonious relationships. In addition, Alvey has enabled different disciplines, different parts of the same firm, and different departments of the same university to work toward achieving common objectives. A few examples of achievements in each of the five main areas of research are:

VLSI

Process Technology

- The EQUIPS package is an interactive process simulator that is now being used and evaluated by the U.K. chip manufacturers STC, General Electric Company (GECO), and Plessey. The process is based on the finite element method of solving differential equation models and covers all major process steps. (VLSI 068)
- The SUPREME II package is a two-dimensional process modeling now used on the production line at STC. The package is a useful aid in the introduction of a new Alvey-supported process in the factory. (VLSI 067)
- The Alvey program 046 has developed optical and electron-beam technology for fabrication of masks and reticles to produce 1- and submicron images accurate to 0.05 micron. The latest Ferranti series of high-speed gate arrays has now used these developments. (VLSI 046)

Whole Process

- Initial exploitation of Alvey 1-micron bulk CMOS whole-process work will be at the new Plessey 6-inch wafer plant at Plymouth. The Alvey 1.5-micron process went into production in early 1989 and is now in full production. (VLSI 059)
- The 1-micron ultrahigh-speed bipolar whole process is being used at Plessey for wide-bandwidth transmission circuits with 10,000-gate arrays and a fast RISC architecture processor. Production began in 1988. (VLSI 061)

- The 1.5-micron Collector Diffusion Isolation bipolar process technology is now in pilot production at Ferranti, with a 2,600-gate array successfully processed. A 40,000-gate chip was produced during the third quarter of 1987. (VLSI 062)
- The 2-micron bulk CMOS whole-process variant of the Alvey 1.25-micron process is in production at STC. The 1.25-micron version is now in full production. (VLSI 071)

Process Equipment

- The enhanced-rate ions etching project for advanced electrode design was useful in developing the Nordiko 4600. This machine provides high throughput and control of etching parameters for very small features. The prototype was completed in July 1987, and systems are priced at £150,000 to £190,000 ($248,000 to $314,000). (VLSI 002)
- The advanced ion etching project has produced a reactive ion etching system giving two orders of magnitude increase in ionization density over existing systems. The prototype has been tested at Plasma Technology. European and American semiconductor manufacturers are interested in the machine, which is expected to sell for about £250,000 ($415,000). (VLSI 013)

CAD Systems and Tools

- Silicon Compiler technology from Lattice Logic has provided fully automatic layout for the first time on Ferranti's new DS series of integrated circuits. (CAD 001)
- The Inmos Ltd. design system, ISIS, first developed for the transputer design, has been licensed to Racal and successfully marketed in the U.S. and Europe. Alvey support has led to a user-evaluation exercise, and various improvements including the ELLA language. The system was used in June 1986 to design the Racal 22K-gate chip, which worked on its first trial. (CAD 010)
- Alvey has supported improvements in the ELLA behavioral language, originally developed by RSRE. In a recent Alvey CAD project, ELLA will be adopted and standardized for all U.K. CAD systems and is currently being marketed in Europe and the U.S. (CAD 002)

Architectures

- The Reconfigurable Processor Array (RPA) achieves improvements in numerical processing speed through parallelism. Parsys and Telmat is marketing the parallel processors in which RPA is used. (VLSI/ARCH 010)
- The study for a transputer supernode is to establish the feasibility of a low-cost, high-performance supercomputer based on replicated clusters of switched transputers. The architecture has been defined and patented, and the specifications for a switch chip have been produced. This work provided the basis for an ESPRIT architecture project--to develop a European supercomputer, which Parsys in the U.K. and Telmat in France are marketing. (VLSI/ARCH 015)

Software Engineering - Software Products

- Eclipse is a set of tailorable software packages to assist in the development of large, complex software systems. Eclipse includes support tools for system design, the ADA language, and the MASCOT design method. The prototype was created in late 1987, and Software Sciences made it commercially available in 1987-1988. (SE 014)
- Aspect developed a prototype integrated project support environment (IPSE) framework which offers a formally defined public tool interface to permit foreign tools to be integrated. A prototype IPSE has been produced. Systems Designers is developing an industrial strength IPSE framework known as Perspective, which will be the vehicle to exploit research results. (SE 001)
- The FOREST language is a specification language and associated method to accelerate and improve the quality of the specification of real-time systems. Modal action logic has been chosen as the specification language, and a method for using it has been developed and support tools written. A full tool set will be available in 1988 and is being used on real products by GECO, the Atomic Energy Research Establishment, and Imperial College. (SE 015)
- The MASCOT software construction system originally developed by Royal Signals and Radar Establishment (RSRE). The Alvey Project has developed an enhanced environment, including building the expertise of experienced designers using an expert systems tool. The prototype is used by Ferranti, Logsys Advanced Systems, and YARD. (SE 044)

- The FORMAT software deals with the application of formal methods to communication protocols, concentrating on OSI standards. The software provides protocol designers with the techniques and tools for effective designing, specifying, verifying, and testing. A specification framework and library is complete and available commercially. (SE 051)
- A tool set and environment for validating programs written in PASCAL is complete; however, some research is continuing. (SE 063)
- A formal definition of the syntax and semantics of the language MODULA2 has been produced with a rigorously verified interpreter. (SE 063)
- The formal specification of GKS, the first ISO-approved computer graphics standard, was completed in April 1987. A detailed specification of the output side of GKS has been produced and work is continuing on the input side. (SE 024)

Systems Architecture - Hardware

- The FLAGSHIP hardware is a parallel architecture optimized for declarative languages and designed as the basis of a range of systems from powerful workstations to large mainframes. The project is based on research at Manchester University and Imperial College of Science and Technology (Imperial), London. Three prototypes have been produced by International Computers Limited (ICL); Manchester, ICL, Imperial, and Edinburgh University for independent evaluation. The complete model of FLAGSHIP became available mid-1988, and ICL expects to market it in the early 1990s. (IKBS 049)
- The GRIP hardware, completed during 1987, is a parallel declarative system but with less demanding objectives than FLAGSHIP. This system provides a modest entry-cost to users wishing to develop parallel declarative applications. (IKBS 065)
- The PARSIFAL hardware is a flexibly interconnected array of transputers, primarily intended as a research and design evaluation tool for simulating parallel architectures. With its supporting subsystem and software, it offers a design prototyping and evaluating service to U.K. industry and researchers. The project has already developed some widely applicable products. Logica has produced an implementation of the Transputer Development System (TDS) on the SUN, which both they and Inmos are marketing. Inmos is developing software to facilitate configuration of switchable networks, which will complement their new switch chips, and which, together with the new low-level multitransputer debugging facilities, will become part of the TDS. (IKBS 074)
- The GAM hardware is an associate memory chip for knowledge manipulation systems. The prototype performed well, and the commercial version was demonstrated in mid-1987. (IKBS 029)
- The CARDS hardware is a content-addressable, relational, database server. Three prototype systems were installed at GECO, Reading University, and the Imperial Cancer Research Foundation during the second half of 1987. The GECO people are evaluating the commercial potential. (IKBS 072)

Software

- The DACTL software is a compiler target language with particular relevance to the requirements of parallel declarative modes of programing. The aim is to reduce the time and cost of implementing and evaluating a range of languages on different host systems. The software is generating interest in the U.K. and Europe in both academic and industrial circles. (IKBS 072)
- The PISA software is a persistent language system with a persistent information space architecture to support this and other persistent languages. A persistent language provides a consistent language interface to all data and functions of whatever persistence, including short-lived data traditionally held in databases. Persistent languages will provide application developers with a simple and consistent language view of all relevant system capabilities, including concurrency, sharing, and distribution. They will insulate application developers from changes in the implementation of these underlying capabilities and allow independent and easier evolution of application and underlying systems. The main output will be a set of rules and guidelines for designers. A reference model became available in 1987, and a large-scale system in 1988. (IKBS 046)
- The Advanced Networked Systems Architecture (ANSA) is an active standards project located on a single site in Cambridge. The ANSA project has developed a networked systems architecture aimed toward a set of world standards for networked systems. The concepts of the architecture is now technically complete and consistent, and documented in the ANSA Reference Manual. The ANSA project has been responsible for several submissions from both British Standards Institute and European Computer Manufacturers Association to the

ISO. Future work will include developing architecture specifications using formal description techniques, evaluating the architecture in the program of implementation projects, and continuing information dissemination to encourage the earliest and broadest adoption of the architecture and its underlying standards. (LD 007)

Intelligent Knowledge-Based Engineering

- Expert Systems for the Design of Spatial Arrangements undertakes ways of representing spatial arrangements and reasoning about these with particular reference to ship layout. A spatial calculus forms the foundation for an experimental system. A numerical design system that was developed in earlier research and will be marketed through Strathclyde University has been incorporated in the system. (IKBS 039)
- The EMEX system is an expert system to assist in the task of building econometric models for market specialists who know their markets but not the mathematics of the models. The first version is nearly completed and a practical package became available in 1987. The system will be extended for use in management training, and test sites for commercial development of the system are under consideration. (IKBS 102)
- The RESCU system is an expert system for quality control of a plant in batch production. The prototype has been installed in an ICI detergent plant. The work resulted in a special language for this type of real-time application and multiprocessor architecture, and led to commercial development of a process control expert system that Systems Designers will market. More than a dozen other systems have been developed and are useful in practical situations. (IKBS 038)

Man/Machine Interface - Human Interface

- Adaptive Intelligent Dialogues explores the potential for accommodating a range of different and developing users by introducing adaptiveness into the Man/Machine Interface. An adaptive interface to the Telecom Gold Electronic Mail service has been designed and built. Document preparation and byproducts already in use are now being researched. (MM/HI 006)
- Alvey centers in London, the Midlands, and Scotland now provide a focus for the human interface community in the U.K., and provide a base to which any organization can turn for training or consulting. Information services are also provided, including the data bank of human interface technology and information on human interface standards. (MM/HI 150)

Speech Processing

- The AUDLAB software, a powerful interactive package to assist in speech recognition and synthesis, was developed at Edinburgh University as part of a speech demonstrator project. This software package has been on the market from UNIVED in Edinburgh since 1987. (LD 006)
- Speech Interfacing and Phonetic Algorithms has developed a single, coherent software package called SPARBASE that manipulates, displays, and analyzes speech. This group of programs is regularly upgraded and is being developed into a general, powerful speech analysis research tool. A method of analysis has been developed that renders better format estimates than any other available. (MMI 009)

Image Processing

- Image Matching for Patient Alignment in Medical Imaging compares images prepared at different times, or with different modalities, to establish accurate repositioning of patients in imaging machines. The work has application in several industries in addition to medical applications, and is being exploited through GECO. (IKBS 053)
- Spatio-Temporal Processing and Optical Flow for Computer Vision enables a computer vision system to obtain a three-dimensional description of visible surfaces and objects in a scene. Since 1987, products have been available for application of these algorithms, encoded in software, to autonomous vehicles or a robot arm. (IKBS 013)

Displays

- The Liquid Crystal Display, a silicon matrix project, produces large, flat, thin color screens with high-information density. The display has a large-area, integrated circuit directly fabricated onto ordinary glass instead of the usual silicon wafer. Because of the Alvey-supported work, a new process and circuit architecture was discovered that has been successfully demonstrated with small, color, prototype displays of up to 40,000 pixels. A competitive product can be exploited by GECO and EEV-LUC for both TV and IT sectors of the market. (MMI 023)

- Interactive Electro-Luminescent Displays has produced an A4-page-size (210 x 297 mm) dc electroluminescent display using improved phosphor powder materials. Also, an interactive half-A4-page display was developed and a demonstrator was built. The display achievements will be exploited by Phosphor Products, with volume production for the business and process control markets wherever space is at a premium and a combined display and keyboard has an advantage. (MMI 130)
- The Ferroelectric Liquid-Crystal Display project has developed a new type of display for high-resolution video images that are not possible with conventional liquid-crystal displays. Considerable progress has been made with a display using ferroelectric liquid crystals. Small test devices have demonstrated that large arrays can be switched at video rates. A good market for this product is expected in the TV and IT sectors through Thorn-EMI and STC. (MMI 131)

Since the completion of the Alvey program, the Department of Trade and Industry (DTI) has determined that all IT work funded by the department will come under one Information Engineering Directorate. This new Directorate oversees projects funded under the LINK scheme described above; research on optoelectronics (JOERS); the existing program of research on gallium arsenide (GaAs) semiconductors; and Britain's participation in ESPRIT II.

Lord Young, former Secretary of State for Trade and Industry, earmarked £29 million to be spent over 3 years on the British programs of IT research to follow Alvey. The British government will contribute £200 million to ESPRIT II. Also, SERC will spend £55 million over the next 5 years on the universities input to the National Research Program.

Mr. John Thyne, head of the Information Engineering Directorate (IED), has a budget for all IT programs in DTI of about £50 million per year (the £29-million Alvey followon is just one part of his budget). Work sponsored by the IED concentrates on electronic devices, including VLSI silicon chips, GaAs, and molecular electronics. A second sector is systems architecture, including parallel processing computers, speech processing, image processing, and communications between computer systems. The third sector covers software engineering, expert systems, and human factors in IT.

Clearly, the British government is in favor of a little more support to European programs like ESPRIT, RACE, and EUREKA as research gets closer to applications and consequently a little less expenditure on applied work in the U.K. However, the next program to be discussed herein, though small, is an example of applied research.

Transputer for Engineering and Science

Introduction

In February 1987, the SERC and the DTI approved funding of £3.5 million ($6.2 million) for a 4-year program on the development of engineering applications of transputer (see *ESN* 40-9:306-309) (see Table 27).

Table 27. Transputer for Engineering and Science Objectives

To promote awareness of the potential of the transputer and associated technology
To enable researchers to acquire the techniques, development tools, and systems software for using transputers in a quick and cost-effective manner
To promote high-quality research using transputers without unnecessary duplication
To transfer the benefits of the research to U.K. industry as early as possible.

The Rutherford Appleton Laboratory (RAL) Engineering Board's Distributed Computing Systems (DCS) program ran from 1977 to 1984. This led to a research community in the U.K. interested in the theory of parallel computing. An important theme of DCS was in loosely coupled distributed systems where many processors could be connected to tackle a specific problem in a flexible way. With large-scale integration, machines could be composed of many self-contained processors, each with its own memory, and could become more powerful and reliable, and cheaper than conventional computers.

In order to use such a machine effectively, it must be possible to program it so that processors can share the work by communicating and synchronizing with each other. The system should be able to cope with the malfunctioning of individual processors. If each of the processors is identical, it will be possible to reconfigure the system and provide a more fault-tolerant system.

Background: Transputers and Occam

In 1978, Professor Hoare, Oxford University, proposed a model of computation called Communicating Sequential Processes (CSP), which concentrated on *input, output*, and *concurrency* as the basic primitives. Messages passed between processes were the basic method of communication, and were synchronized so that the sender waits until the message is received.

Using these concepts, Inmos Ltd. developed a microcomputer--the transputer--designed for building high-performance computer systems. Inmos also designed a language--Occam--which implements Hoare's CSP theory (see *ESN* 40-9:306-309). The transputer can carry out a set of concurrent processes with special instructions sharing the processor time between the concurrent processes and perform interprocess communication. The transputer's external behavior corresponds to a process so that transputers can be linked with interprocess communication in a way similar to communication inside an individual transputer. Occam defines the computation to be performed as a collection of concurrent processes communicating with each other through channels. An Occam program can be executed by a single transputer, a small network of transputers, or a much larger network. Since a collection of processes is itself a process, an application can be defined hierarchically with a manageable set of processes being defined at each level.

The RAL people are providing support for an Alvey-funded research project, *The Transformation and Verification of Occam Programs*, between Oxford University and Inmos Ltd. Since Occam is derived from Hoare's CSP, it is possible to define a set of laws between Occam programs, which can be used as the basis of an automated transformation system. Transformations of the original program can be defined, guaranteeing that the new program has the same meaning as the original one. This can be used for improving the efficiency of the program to show that two programs are equivalent, and to transform to a restricted syntax for VLSI implementation. A prototype system has been written in the Edinburgh Standard ML language which can transform Occam programs to a normal form.

Publicity has been an important component of the initiative and a regular mailshot has been established with 800 currently on the mailing list. In April 1987, SERC formally announced the approval of the first phase of the initiative. Also, members of the coordination team have given several invited talks at conferences and other meetings, and in all cases, the initiative has been enthusiastically welcomed.

Occam User Group

The Occam User Group (User Group) is an informal organization run by its own members. The Occam programing language, developed by Inmos, is its primary concern, with the hardware of the transputer a secondary area of interest. The User Group is a forum for the interchange of information among existing and potential transputer and Occam users, and is a channel for communication with Inmos. These aims are met by meetings, a newsletter, and the exchange of programs between members. Technical meetings are held biannually, in March and September. The meetings include informal presentations and demonstrations by members and by Inmos. There are special interest groups in AI, learning, operating systems, formal aspects, networks, transputer hardware graphics, numerical methods, and the UNIX operating system. The User Group maintains a catalogue and allows members to publicize programs that they are willing to share through the newsletter.

Edinburgh Concurrent Supercomputer

The Edinburgh Concurrent Supercomputer (ECS) is a multimillion dollar installation, built by Meiko Ltd. and based on transputers. It is supported by DTI, the Computer Board, SERC, and industry. The ECS is a large reconfigurable array of Inmos floating-point transputers, with several hundred megawords of fast memory and a distributed file system, providing supercomputer performance. Also, it is suitable for a wide range of applications.

Future Activities of the Engineering Applications Initiative

The most urgent requirement is to bring the regional centers up to their full operational level as quickly as possible. This is to ensure that the impact on U.K. industry will begin to take effect in 1988-1989 and beyond.

On April 1, 1988, associated support centers were introduced. Eight such centers were established during 1988-1989 with the Future Activities of the Engineering Applications Initiative (Initiative) contributing equipment, but no manpower. The Daresbury Laboratory has already been established as an Associated Support Center to ensure maximum cooperation between the Initiative and the work at Daresbury on the Floating Point System T-20. The Initiative has provided a limited-configuration Meiko machine. Software developed for the T-20 will be ported to the Meiko machine and will be made generally available to the engineering community. As part of this arrangement, engineers can also have access to the T-20 systems.

The Loan Pool will be increased in both size and range of software and hardware offered. Many new developments have occurred since the start of the program; e.g., announcement of the T800 Floating Point System T-20. However, limited funds have restricted the range of equipment currently offered. The policy will continue of providing only commercially available products. Further and extended development contracts will be awarded to ensure the usability of multitransputer systems in real applications. This will ensure use of these systems by U.K. industry.

Participation in European Programs

ESPRIT

The U.K. has been a very active participant in European R&D programs. Despite the substantial commitment to the Alvey program, (which began before ESPRIT and involved a £200-million U.K. government commitment); 66 U.K. companies and 35 U.K. universities were active in ESPRIT I. France had one more company in ESPRIT I than the U.K., but 10 fewer universities. Apart from France, the U.K. substantially exceeded all other countries in both company and university participation.

The 5-year U.K. commitment to ESPRIT II is £200 million. This is £65 million more than that recommended by the Bide Committee which was appointed to recommend a followon to the U.K. Alvey program.

EUREKA

The U.K. is involved in about 36 percent of EUREKA projects.

RACE

During the RACE Definition Phase, completed in 1987, in-depth studies were made in 35 different sectors of R&D. British companies participated in 26 of these studies.

Federal Republic of Germany

The FRG, like other European nations, has moved much more slowly toward privatizing and liberalizing than has the U.K. Nevertheless, the FRG administration is aware of the impact of combining telecommunications and information services; e.g., combining the services of a traditional monopoly with those of a nonmonopoly. This, together with awareness of increased user needs and demands for additional services and more flexibility in its provision, has caused the FRG government to reassess its traditional position. They are aware of the need to work with the user community in order to find the best solutions to user problems and needs. The government is beginning to realize that some competition among equipment and services suppliers may be desirable.

In 1987, Professor Eberhard Witte, Munich University Institute for Organization, completed a study and made several recommendations concerning a comprehensive reorganization of the telecommunications market and service. His study recognized the two-thirds parliamentary majority that would be required to change Article 87 of the basic law governing the operation of the Deutsche Bundespost (DBP).

Competition is already allowed in a range of terminal devices and in data communications. Professor Witte recommends that all equipment that uses terminals, including the telephone, be a completely liberalized market. He also recommends that any private supplier should be permitted to offer any and all auxiliary telecommunications services (nonbasic services). Such services should be subject neither to authorization nor to registration with the DBP. Professor Witte recommends that the installation and further development of the infrastructure covering the entire country should continue as the responsibility of the Federal government.

The telecommunications services of the Federal Postal Administration (to be called Telekom) should meet government requirements for complete area coverage of the country. Telekom should also provide a unified scale of charges, equality of customer treatment and sufficient safeguards to meet emergencies and the needs for national defense. As a result, Telekom would continue to exercise a monopoly over the telecommunications network. However, private companies, said Professor Witte, should be assigned leased transmission lines on appropriate and competitive terms. If this is not done during a 3-year trial period, he recommends that the network should be opened to competition.

The telephone service, as the pure transmission of oral language, should remain a state monopoly. However, not the combined services of text, picture, or data transmission which include oral language as well. If adopted, this would lead to a further reduction in the state monopoly with the introduction of ISDN.

An important part of the proposed change would be the separation of legislative and administrative tasks from the organization and use function (Telekom). The former may not, under present law, be subordinated to the rules of free enterprise. Under the plan, Telekom would be headed by a management board of directors. That arrangement would not raise any constitutional problems.

Because of the different paths in their technical development and demand for differing entrepreneurial concepts, the postal services and the telecommunications service should be separated, says Professor Witte. His study recommends the transition in telecommunications to customer relations under private law to place suppliers and customers on an equal legal footing. Rather than blindly copying liberalization measures adopted abroad, says Professor Witte, the FRG should find its own solution which forms a basis of all its considerations, where politically feasible.

The recommendations of the study were implemented at the beginning of 1990. There is a Postal Services Company, a Postal Banking Services Company, and a telecommunications company called Telekom. Competition is allowed in Customer Premises Equipment and in VAN services.

In recent years, the German government is playing a more important part in R&D in the computer, or IT, industry, and in the electronics industry.

Federal Republic of Germany National Programs

Suprenum

Suprenum is the supercomputer being developed under the leadership of Professor Wolfgang Gilio, head of the Berlin branch of Gesellschaft für Mathematik und Datenverarbeitung (GMD). The name Suprenum is the diminutive of Superrechner für Numeriche Anwendungen. Suprenum is partially funded by the German Ministry of Research and Technology (BMFT). Four industrial partners (Suprenum GMbH, Dornier GMbH, Krupp Atlas Elektronik GMbH, and Stollmann GMbH), five research institutes and five universities are involved in various aspects of the hardware and programing development. The 1989 goal for Suprenum 1 was to produce a 256-processor unit system with a performance of 1-5 Gigaflops. Suprenum was demonstrated at the Hannover Fair in 1989 with a 32-node system.

In Suprenum, the designer chose a multiple instruction stream, multiple data stream (MIMD), multiprocessor system with local memory and a vector floating point unit in each node. A cluster consists of 20 nodes, accommodated in one 19-inch rack. There are 16 working nodes, a standby for fault tolerance use and three specialized nodes for the cluster disk controller, the intercluster communications node, and the cluster diagnosis node. In the prototype system, there are 16 clusters. The architecture is a two-level bus-coupled architecture with the 16 working nodes in a cluster connected by a clusterbus; the clusters are also bus connected. Communication between the processors is by message passing.

The clusters communicate through an interconnection structure consisting of a matrix of bit serial ring buses. Each such ring bus has a gross data transmission rate of 280 million bytes/second, resulting in a net data rate of 25 million bytes/second. The protocol employed on the ring buses is a version of the slotted ring protocol (Giloi). Each cluster can be reached through two such buses--a row bus and a column bus. This doubles the interconnection bandwidth and renders the interconnection structure fault tolerant. The intercluster communication is able to perform an alternate routing in the case of a permanent bus fault. Transient faults are detected and masked through retransmission by the slotted ring protocol. The intercluster communication node is capable of handling the entire protocol hierarchy that regulates the exchange of packets or larger logical entities consisting of several packets. The intercluster communication node consists of a microprogramable flow control unit to handle the higher levels of the internode communication protocol, some fast buffer memory, and a set of proprietary ECL gate array chips to handle the lower levels of the slotted ring protocol.

In a node, the memory is 8-Mbyte RAM and the CPU runs at 2 Mips on a Motorola chip. The vector unit is a Weitek chip set 2264/2265 which operates on vectors of 64 bits with a speed of 8 Mflops (for dot products this increases to 16 Mflops), and there is an 8-K word vector memory.

Suprenum is a multipurpose computer for large-scale scientific computing problems, which are generally characterized by grid structures. Multigrid is a very important but special approach. However, any other grid and mesh application and matrix calculations should run efficiently on Suprenum when suitably partitioned.

Languages to be supported by Suprenum include Fortran, Modula-2, and C. From the users viewpoint, the operating system is UNIX, which runs the front-end computer. The Suprenum nodes run a basic operating system--PEACE--which communicates with UNIX. An integrated graphics system will be offered, usable in pre- and postprocessing and during processing to visualize the applications and their results and for system diagnostics.

Portability of software is a general goal of the system and a communication library for grid problems has been developed. If the programer uses the subroutines of this library, his program becomes independent of the machine at hand.

Suprenum 2 is being planned using new technologies for a larger system with up to 4096 nodes.

The Mega Project

In 1983, the BMFT became concerned about several strategic growth areas, a prominent one being microelectronics. During the same year, they made a study trip to Japan and invited Siemens and Philips to send representatives. As a result of what they saw in Japan, Siemens, and Philips agreed to cooperate developing of two different memory chips. Siemens would concentrate on the 4-megabit dynamic RAM and Philips would work on the 1-megabit static RAM. Work began on the overall plan for the Mega Project in November 1983, and by June 1984 details of the plan had been agreed upon. The FRG government agreed to supporting the project with DM320 million and the Dutch government agreed to contribute DM160 million. Siemens and Philips then paid DM1.4 billion for developing and DM1.5 billion constructing production facilities.

The project represents an unprecedented effort in Europe to overtake the Japanese and Americans in mass-produced microchips, who are at the heart of both the computer and the telecommunications industries. In effect, the Mega Project is designed to compensate for the estimated 2-year deficit over a 5-year period. To accomplish this, research, development, and preparation for production must proceed in parallel rather than successively.

Since impurity can be fatal in chip production, processing spaces can contain at most one dust particle larger than 0.5 micron/ft^3. That means the air in the spaces must be changed 500 times each hour.

By March 1987, a prototype 4-megabit chip was produced, less than one square centimeter in size. The individual circuits on the chip are only 0.8 micron wide. Ditches one micron wide and four microns deep are drawn in the chip, and memory circuits are put onto the walls of these ditches. Volume production of the 4-megabit chip began in 1989.

Siemens and Philips plan to cooperate on developing the generation to follow the 4-megabit chip which is expected to be a 16-megabit chip. The two firms are working together on x-ray lithography that should permit 0.4-micron circuit width on a chip. The Mega Project is being subsumed under the JESSI program, a part of the EUREKA program, previously described.

Participation in European Programs

ESPRIT

The FRG has been one of the three very active participants in the ESPRIT program (with 54 companies and 25 universities participating) and a strong commitment to ESPRIT II. The U.K. and France are the other participants.

EUREKA

The FRG is active in about 33 percent of EUREKA projects.

RACE

During the RACE Definition Phase which was completed in 1987, in-depth studies were made in 35 different sectors of R&D. Companies from FRG participated in 19 of these sectors.

France

Like other European governments, the French government is playing a more important part in R&D in the computer, or IT, industry, and in the electronics industry. The speed with which France moves toward liberalization in the telecommunications industry is, to some degree, a function of which political party is in control of the government. On the technological side, France has moved very quickly and now has more than 50 percent of its telephone lines on digital switching and most of its long lines in fiber optics. After the May 1988 elections, Mr. Paul Quiles was appointed Minister of Post, Telecommunications, and Space (PTE) replacing Mr. Girard Longuet.

In a speech in London in December 1988, Mr. Longuet asserted France's "political determination to work enthusiastically towards a Common European Telecommunications policy and remain a driving force behind all common ventures." He then described three important programs that he had initiated (see Table 28).

Table 28. Minister of Post Programs

1. In cable networks, he abolished the DGT's monopoly and created a competitive environment based on real operating costs.
2. With respect to paging in radio communications, he authorized two competing operators to enter the market and they quickly launched operational services. For radio telephone, he issued tenders for a second national operator alongside the DGT.
3. In Valued Added Services, he said "my aim is to create conditions in which the DGT and our companies can develop an offensive strategy in the world's markets, notably through a series of alliances."

Apparently, Mr. Quiles will mainly follow the policies laid down by Mr. Longuet but at a much more measured pace. He then gave the three main goals of a White Paper issued in 1987 (see Table 29).

Table 29. 1987 Minister of Post Goals

1. The separation of telecommunications operators from the function of regulation. The supervisory function will be split between the State and an independent authority, the CNCL, on the lines of the FCC in the U.S.
2. Confirmation of the rule of competition in telecommunications services other than the transparent transfer of information as well as laying down precise rules for the public service tasks of the operator or operators authorized to establish such open transparent information transfer services.
3. The need for autonomous status for the DGT, which is having to contend with competition abroad, and soon too in France, rendering its present status as a government agency totally unsuitable.

In a press conference on July 19, 1988, Mr. Quiles declared his intention to retain the competition introduced by his predecessors in mobile telephones and paging. He also said that the recent value-added decree would remain in effect. He called deregulation.."a worldwide movement which cannot be denied and is inevitable." But he said he opposed what he termed *savage* deregulation. He called for a strong IT that could resist the attacks coming from Japan and the U.S. One way of achieving this goal is to assure that the IT has reserved profitable areas of activity. He called for a European response to foreign competition. He said it is important for the Europeans to control basic services such as the transport network.

Mr. Quiles also said that changing the status of PTE was not a top priority. There is to be no immediate change in the civil service status of the 300,000 PTE staff. He said, however, that one of his most important goals would be to create an independent regulatory body.

Nevertheless, in a move similar to that taken by Spain and the Netherlands in January 1989, and by the FRG in January 1990, France proposed in early 1990 to institute France Telecom to handle telecommunications and the French postal organization to deal with postal matters, as autonomous public establishments. However, a difference from the

arrangement in Spain, the Netherlands, and the FRG will be retention of civil service status and social guarantees for the staff.

To take account of trade union wishes that the PTT Ministry should continue to have overall responsibility for employment matters, a public interest group (GIP) is expected to be set up, supervised by the ministry. The group would manage the services common to France Telecom and the postal organization as well as employment matters.

The boards of the two establishments will be set up with participation from government, political personalities, and staff representatives. The staff representatives will be elected as in other public enterprises and each of the three categories would be equally represented. The political section would include members of parliament.

At present, France Telecom has debts of 119 billion Francs, which puts it at a disadvantage with respect to its European counterparts. How to handle the debt problem is under discussion.

French Research

The Institute National de Recherche en Informatique et en Automatique

The Institute National de Recherche en Informatique et en Automatique (INRIA) was founded in January 1980 under the Ministry of Research and Industry and has four missions (see Table 30).

Table 30. INRIA Missions

1. Accomplish fundamental research and its applications
2. Realize experimental systems, notably in association with public and private laboratories
3. Organize international scientific exchanges
4. Assure the transfer and diffusion of knowledge and expertise on a national basis.

The three main laboratories of INRIA are at Rocquencourt (near Versailles), Rennes, and Sophia-Antipolis, and has eight principal themes of research (see Table 31).

Table 31. INRIAs Principal Themes of Research

1. Modeling and numerical logic
2. Automation systems
3. Data processing, images, and robotics
4. Algorithms and programing
5. Languages and specifications
6. Computer science systems
7. Man-Machine communication
8. New architectures and specialized machines.

A few examples of research at INRIA-Rocquencourt are discussed herein.

The 802.3D Protocol. A Variation on the IEEE 802.3 Standard for Real-Time LANS (based on discussion with Gerard LeLann). Token-passing LANS have limited flexibility and robustness capabilities. In noisy environments or when system configurations must be transparently modified, it may not be feasible to predict token-passing LANS behavior or performance. Alternate solutions are contention schemes that are often assumed to be probabilistic. Overly simplified statements continue to be propagated and trusted as in the labeling of token-passing LANS (802.4 and 802.5) as deterministic and contention LANS (802.3) as probabilistic.

Determinism is a logical concept; i.e., making use of a deterministic algorithm does not mean that given timing constraints will always be met. Many parameters have to be considered to compute the exact physical values of expected upper bounds. If these values are too high, then determinism does not help.

Because contention protocols belong to the family of random access protocols, they are regarded as behaving probabilistically. One might believe there is only one way to resolve collisions--the ethernet way. Although the Binary Exponential Backoff algorithm is of a probabilistic nature, it is wrong to state that contention LANS must be probabilistic in general. The fact that initial accesses can lead to collision does not necessarily mean that contention schemes must be probabilistic.

The interest in deterministic contention LANS is so high that prototypes have been built or are being built in France, Germany, the Netherlands, Israel, Japan, and the U.S. The potential commercial success of this approach lies in the low prices reached by contention access units. If physical intervention needed to implement a deterministic collision resolution scheme is limited in complexity and cost, then deterministic 802.3-like LANS could be on the market reasonably soon. Such LANS could guarantee that all messages involved in a collision are transmitted in some bounded finite time. Therefore, such LANS could be used to carry all kinds of traffic mixes such as aperiodic data packets and periodic voice or sensor packets.

The 802.3D protocol is a deterministic contention Medium Access Control (MAC) protocol consisting of five properties (see Table 32).

Table 32. Medium Access Control Properties

1. Fully compatible with the IEEE 802.3 Standard, currently the most popular standard for open LANS. In particular, the 802.3D protocol is compliant with the IEEE 802 and the ISO/OSI standards for layers 1 and 2 (physical and link) interfaces
2. Independent of the type of physical medium used, provided that the physical layer implements an interface with the MAC layer which complies with the IEEE 802 and the ISO/OSI 8802 Standards
3. Guarantees finite-bounded delays
4. Retains the flexibility and robustness properties inherent in the IEEE 802.3 Standard
5. Ensures efficient handling of various mixes of periodic and aperiodic traffic flow.

Binary tree search is used to resolve collisions deterministically. This type of algorithm is known to be optimal in the absence of information with respect to which and how many traffic sources are involved in collision. Two collision resolution options are available--the general mode (full tree search) and the cycle mode (leaf search).

An 802.3D network has two modes with respect to access policies, random, and epoch. The random access mode is strictly equivalent to the IEEE 802.3 standard. Transition to the epoch mode occurs automatically when a collision is experienced. Every message involved in a collision is transmitted within the subsequent epoch. Transition to the random access mode occurs automatically at the end of every epoch.

Within an epoch, two options are available. Namely, (1) the blocked entry mode in which only those messages involved in the original collision can be transmitted within an epoch; and (2) the free entry mode in which any station can transmit a message within an epoch provided it can do so according to the tree search process. The tree search process is conducted in parallel by all stations. A channel phase can be a successful message transmission (x), an empty channel slot ( ), or a collided channel slot (c).

At the MAC layer, every message is associated with a unique identity or name. A name (and therefore a message) is unique. A name (and therefore a message) corresponds to one of the tree leaves. Two mapping options onto physical network stations are available, single naming (one name per station) and multi-naming.

If X is the set of names, upon occurrence of a collision while the channel is in the random access mode, every station divides set X into two subsets. Subset W includes the winning names; i.e., the names designating those stations that are allowed to try again at the end of the channel phase corresponding to the collision. Subset L includes the losing name; i.e., names designating those stations that must refrain from transmitting until all messages pertaining to subset W have been successfully transmitted over the channel. Every station monitors the channel to follow the tree search process, including inactive channels. Every subsequent collision, within an epoch, results in the same splitting process being applied onto the current subset W.

When it can be predicted that a channel will be highly loaded or when stations exhibit a cyclical behavior, it might be appropriate to save the overhead incurred when starting the tree search from the root of the tree. Rather, a leaf search is recommended, which is equivalent to a conventional asynchronous contention scheme, and just a particular variation of the general mode. The distinction between the general mode and the cyclical mode is made through the

choice of an appropriate initial value for a parameter that represents the height of the tree to be searched. The resultant behavior under the cyclical mode is a succession of epochs separated with a collided channel phase.

Every station must be allocated a unique name. Physical addresses should not be used as names. Under the single naming option, every station is allocated one name only; whereas, under the multinaming option, every station can be allocated several names. The selection of a name for a given message can be based on dynamically available data, such as message priorities. In order to conduct the tree search, a station only needs to know its names and the current channel state.

When a station is powered on or when a station is reconnected to the medium, some time must elapse before this station is synchronized with other stations. The upper bound of this wait interval is equal to $k + 1$ epochs of maximum duration, where k is such that the number of allocated names is between 2^{k-1} and 2^k.

Test results show the following:

- The 802.3D protocol under general mode is well adapted to handling light and medium loads or long frames and is insensitive to the number of traffic sources as well as load distribution. However, performance degrades sharply near channel saturation.
- The 802.3D protocol under cyclical mode is better adapted to the handling of high loads and/or short frames, leading to quasi-fully used epochs. The protocol is sensitive to the number of traffic sources.
- The 802.3D protocol can be further improved by complementing it with a few simple mechanisms similar to those used with the 802.4 protocol.
- For every scenario, there is always an 802.3D functioning mode which achieves better performance than either the 802.3 or the 802.4 protocols.

U.S./Europe Gateway Development and Protocol Harmonization (based on a paper by L.H. Landweber). There are three components of this work (see Table 33).

Table 33. U.S./Europe Gateway Development and Protocol Harmonization

1. U.S. academic network participation in the RARE OSI harmonization activity in Europe
2. Specification, design, and implementation of an OSI transport/network level gateway to connect academic networks in the U.S. and Europe
3. Support for medium bandwidth satellite links between European academic networks and the NSFNET.

The Research Associes pout la Recherche European (RARE) organization was formed in 1984 for coordination of national academic networking activities in Europe. The need to facilitate cross-border communication was recognized as was the need to avoid incompatibilities in communication protocols. The objectives were: (1) exchange experience of various networking organizations, (2) establish information and directory services, (3) plan gateways between existing networks inside Europe and gateways outside Europe, (4) harmonize protocols while conforming to ISO/OSI standards, and (5) accelerate the ISO/OSI product availability.

The U.S. has the same concerns. In the U.S., there are existing academic networks including BITNET, CSNET, ARPANET, and UUCP, as well as a wide variety of new networks (state, regional, consortium, pilot) being established under the umbrella of the NSFNET activity. Adopting transmission control protocol/internet protocol (TCP/IP) by NSFNET and its affiliated networks, together with projects exploring the use of these protocols in BITNET and CSNET, ensure that the U.S. nets will be compatible. There is also interest in the U.S. in eventual migration of networks to new protocols being developed by the ISO. The DOD and the NSF, among others, are committed to an eventual migration to ISO protocols.

The RARE organization is responsible for coordinating the use of ISO protocols when available by the European academic and research communities, and for planning gateways to networks outside Europe. The U.S. networks will participate in RARE as liaison members and as such may send observers to the RARE Council of Administration. They may also participate in the activities of the various working groups. The U.S. RARE liaison will come from CSNET and BITNET. Suitable individuals will be chosen at the appropriate time to participate in RARE technical working groups.

There is a serious incompatibility between the U.S. and European approaches at the network and transport levels of communication. In the U.S., a connectionless network protocol combined with a reliable connection oriented-transport protocol (TP-4) will be used. In Europe, a reliable connection oriented-protocol (X.25) is to be used with a *lightweight* transport protocol (TP-0). Both have advantages and disadvantages and neither side is likely to switch to the other's approach.

The plan is to develop a gateway that will provide for translation between the two systems. The gateway will have to translate routing, address information, and maintain virtual circuit state information in both directions. The research will be done by network groups at the University of Wisconsin (Wisconsin), and at the CNUCE Research Center in Italy, and the INRIA Research Center in France.

The Wisconsin group is involved in an ISO implementation project of Berkeley UNIX on the IBM RT/PC. This includes ISO network and transport protocols for the gateway as well as session, presentation, file transfer (FTAM), and electronic mail (MHS) protocols. An earlier project at Wisconsin involved implementing of the DOD protocol suite TCP/IP and associated application protocols for the IBM VM system (WISCNET). This software is used by about 100 universities worldwide.

The CNUCE is working on OSIRIDE and OSI/LAN. The OSIRIDE team is to create a computer network for the Italian science community. The OSIRIDE team also has specified a subset of available services and protocols for transport, session, FTAM and MHS, and protocol implementations are working at pilot centers with connections to ITAPAC, the Italian X.25 public data network. The OSI/LAN is creating an ISO/OSI environment on IBM PCs attached to a token ring.

At INRIA, several teams are working on new network protocols for new applications, including cooperation between supercomputers and workstations and real-time transfer of voice and images. The INRIA has several researchers engaged in OSI-related activities. As of September 1987, satellite links were installed between the U.S. and Italy/France to enable 64 kbps ISO based end-to-end communication between the Italian/French networks and NSFNET (see Table 34).

Table 34. NSFNET - Italian/French Satellite Links

The satellite links will
Provide scientists in each country with immediate access to supercomputer resources in the other countries based on use of INTERNET protocols (TCP/IP)
Provide a testbed for the U.S./Europe OSI gateway and for other experiments with ISO protocols
Provide an OSI-based communication path for collaboration in science.

The plan is to use half the bandwidth for immediate supercomputer access and collaboration in science and the other half for continuing development of the OSI gateway. At present, TCP/IP is being operated over the supercomputer access/science collaboration component and the other half is used for development. When OSI-based services are fully available on the NSFNET, the entire bandwidth will be used for ISO protocols.

Introduction of Symbolic Problem-Solving Techniques in the Dependence Testing Phases of a Vectorizer (based on the work of A. Lichnewsky and F. Thomasset). The purpose of a vectorizer is to perform program restructuring to exhibit the most efficiently exploitable forms of vector loops. In order to restructure loops for vector or parallel execution, it is essential to obtain very detailed information on the data and control dependencies between multiple indexed occurrences of instructions. Generally, the original instructions are contained in a nested set of loops, which provide indexed sets of instruction occurrences. The investigator looks for a different order of execution of these occurrences, permitting the parallel or vector execution of some loops, while retaining the original semantics. Dependence analysis must be capable of accounting for subscripted variables, and exploiting available information on index variation and range.

The approach used at INRIA is to use the VATIL vectorizer to combine two classic approaches:

(1) Methods have been derived to determine subscripted data dependence by reducing subscript expressions and loop index variations to appropriate arithmetic criteria. The extension is used of such techniques to the cases where variable aliasing and reshaping are permitted.

(2) Methods have been developed to solve decidable classes of sets of symbolic equations and inequations, as well as to approximate intractable problems by simpler ones, which can be solved algorithmically, yielding some approximate information. The feasibility of approximation relies on the problem-related fact that it is safe to replace a problem by a new one having a larger set of solutions, when the parallelization criteria possess the property of monotoncity. However, some vectorizable statements may fail to be vectorized.

Combining the above two methods is achieved by evaluating some of the classical criteria symbolically when it explicitly cannot be done numerically. Then, one endeavors to disprove the resulting set of predicates in the context of the available semantic information using approximate decision methods of procedure (2) above. This enables staying close to well-known criteria, which have been specifically optimized for the purpose of a vectorizer, and yet not limited by their classical numerically explicit implementation. The choice used from procedure (2) problem-solving procedure, was the Sup-Inf method of W.W. Bledsoe described in *A New Method for Proving Certain Presburger Formulas*, 4th International Joint Conference Artificial Intelligence, Tblissi, U.S.S.R. September 1975. This method has a high level of generality but requires some form of computational complexity control in the case considered. Within the Lelisp written implementation of VATIL, which uses symbolic oriented routines heavily, the existing programs have been extended to collect symbolic equations rather than signal failure to evaluate explicitly. The techniques are extendable to use information collected by other methods as well.

A major difficulty is that the general symbolic systems that can be generated potentially cannot be decided or are impractical because of their high computational cost. Thus, one relies on the fact that approximations can be made safely, and on the adapted construction of the required symbolic systems. The overall efficiency of the approach is due to the use of costly generalization, only when classical criteria have failed. Even in such cases, the overall efficiency is further increased by starting from well-adapted generalized versions of these specific arithmetic criteria.

Participation in European Programs

ESPRIT

France has been about as active in ESPRIT as has the FRG. Both have fallen slightly below that of the U.K. France had 67 companies and 25 universities participating in ESPRIT I.

France also has a strong commitment to ESPRIT II.

EUREKA

The EUREKA program was started at the instigation of President Mitterand of France. France is active in about half of EUREKA projects.

RACE

During the RACE Definition Phase, which was completed in 1987, in-depth studies were made in 35 different sectors of R&D. France had companies in 26 of these sectors, sometimes as many as four or five companies in a single sector.

Italy

Telecommunications

In early 1989, a cooperative agreement was entered into by AT&T and Italtel, the largest telecom equipment manufacturer in Italy. The agreement addresses cooperation in R&D and a share for AT&T in the Italian telecom network equipment and services market. This should give AT&T about a 10 percent share in Italy's $4-billion telecommunications market. Until late 1987, there was a plan underway to combine Italtel, a subsidiary of STET (Societa Financiaria Telefonica) and Telettra, a Fiat subsidiary in joint venture company to be called Telit. However, the difficulties of combining a privately and a state-owned company led to Fiat's withdrawal from the planned venture in late 1987.

A holding company in the telecommunications and electronics sector, the majority of STET's shares are owned by the state organization, IRI. The companies of STET are active in telecommunications services, telecommunications and electronics manufacturing, and IT services. Companies of the STET group operate about 80 percent of telecommunications services, and the Italian government directly operates part of the domestic long distance service, service within Europe, and telex service.

The Italian government intends to enact legislation that would concentrate all telecommunications operations controlled by private companies acting as licensees, while retaining for the state the function of regulation, supervision, and control. The present Italian telecommunications services include: 19 million telephone subscribers, a 33.3 percent telephone density, 46,000 facsimile subscribers, 20,000 radio paging customers, 18,000 mobile radio customers, 10,000 videotel customers, and 244,000 data transmission users.

The Italian telecommunication service suffers from several shortcomings: low level of density of basic services, quality of service (especially in large cities) readiness to satisfy the basic demand, slow to introduce new services, and lack of harmonization among different geographical areas.

Italy's "Plan Europe" aims to reach the level of service of other European industrialized countries (see Tables 35 and 36).

Table 35. Italian "Plan Europe" Objects

Penetrate telephony widely to reach the level foreseen in 1992 in the U.K. and already reached in France and the FRG
Accelerate renewal of existing plants and improvement of network performance
Reduce waiting time for service access
Reduce repair time
Diffuse modern telephone equipment
Diffuse radio-mobile services
Enhance residential users services
Implement optical fibers and satellites for transmission.

Table 36. Italian "Plan Europe" Expectation

5 million new telephone subscribers by 1992
4 million electromechanical line renewals
250,000 radio-mobile subscribers by 1992
640,000 data transmission installation by 1992
6,000 additional employees
1 defined set of parameters for the quality of service
$8.5 billion additional investment for the current plans.

Semiconductors

Like other major European countries, Italy has recognized the importance of the semiconductor business in the IT and telecommunications businesses. Italy's main computer company is Olivetti.

In 1987, the Italian company, SGS, and the French company, Thomson, formed a joint company called SGS-Thomson (ST) under the chairmanship of Mr. Pasquale Pistorio of SGS. In merging, ST closed or sold five factories, reduced its workforce by about 2,000, and reorganized its production by shifting some 100 processes.

The company achieved an operating profit of $500,000 in the second quarter of 1988, following a loss in 1987 of $200 million and a loss in the first quarter of 1988 of $10 million. Sales in 1988 for ST reached $1 billion, making it the 13th largest semiconductor producer in the world, taking about 2.7 percent of the global market. Productivity has increased. At the time of the merger, ST was generating $44,000 in sales per employee; the figure is now $62,000. The company

employs 17,000 people. The company intends to expand its product line to include DRAMs and microprocessors, hoping to raise the company turnover to $2.5 billion by 1993.

Through the purchase of the U.K. company, Inmos, ST became an important producer of microprocessors. The Inmos transputer is playing a major role in European computer development.

Italian Research

The Italians are active in most areas in telecommunications, computers, and microelectronics. For example, the Italian research center, CNUCE, participates in the U.S./Europe gateway development along with the American NSF and the French INRIA. This work was described in the previous section on France. In this section, I discuss work on Solid-State Electronics, Information Systems, and Parallel Computing.

Solid-State Electronics at Consiglio Nazionale delle Ricerche

In 1970, the Institute of Solid State Electronics of Consiglio Nazionale delle Ricerche (CNR) began its work. The CNR has concentrated on the development of devices based on advanced research and technology. One objective has been to establish working relations with the science community and with industry.

Solid-state electronics deals with the close interaction between rapidly developing science and the growing market, with continuous exchange of information in both directions.

The CNR's main areas of activity are: Magneto-Optic, Structured Analysis of Materials, Chemical Sensors, Microwave Materials and Devices, Biomagnetism, Electron Beam and X-ray Lithography, Superconducting Devices, and High-Temperature Superconductivity. Each of these fields is briefly described in the following paragraphs.

Magneto Optics

Named for Faraday and Kerr, the relevant magneto-optical effects are the rotations undergone by the polarization plane of a light beam traversing, or reflected by, a longitudinally magnetized sample. The study of magneto-optical effects enables the fabrication of several devices that exploit magneto-optical effects. These are used in displays, printers, active elements for integrated optics, reading heads for magnetic recording, and magnetic field measuring systems. In most cases, the base material of such devices belongs to the family of magnetic garnets, employed both as bulk crystals and as epitaxial films. One can vary several physical properties of garnets, to a large extent and in a controlled way, by changing their composition or subjecting them to appropriate postgrowth thermal treatments.

For more than 15 years, the CNR of solid-state electronics has been active in magneto optics. Garnets of several compositions have been studied using a technique called Angular Variation of Induced Anisotropy (AVIA). The technique is very effective in unambiguously identifying the crystal sites occupied by the magneto-optically active ions.

The CNR has invented and patented a new kind of magneto-optical display, and is now involved in a multiyear program dealing with the realization of bulk and epitaxial materials to be used in some devices as magneto-optical isolators and deflectors. The CNR cooperates with the University of Hamburg, FRG, for the realization of Mossbauer Monochromators, garnet films enriched with the isotope Fe^{57}, able to extract radiation from the synchrotron light. This will make an x-ray source extremely monochromatic and collimated, and of great interest for studies of physics, material science, chemistry, and biology.

Structural Analysis of Materials

An accurate structural analysis of thin films and interfaces is required for the complete understanding of these phenomena and for the realization of more effective devices. Several techniques have been set up for thin films studies, mainly based on x-ray diffraction and Mossbauer spectroscopy. The activity has mainly been directed toward the study of epitaxial films of garnets, III-V heterostructures, x-ray standing waves, synchrotron radiation, and Mossbauer spectroscopy.

When a garnet film is subjected to ion implantation or to thermal treatment in reduced atmospheric pressure, a thin layer is formed on top of the film with structural and magnetic properties modified with respect to the underlying film. A characterization of these thin film layers was carried out by double-crystal x-ray diffraction and conversion electron Mossbauer spectroscopy. The possibility of replacing the ion implantation by simpler thermal treatment to obtain thin layers with a different orientation of magnetization is the subject matter of an approved patent.

In collaboration with the Department of Electrical Engineering of the University of Colorado, Boulder, III-V heterostructures grown by Metallic Oxide Controlled Vapor Deposition (MOCVD) have been studied. Structural characterization of $Ga_xa1_{1-x}As$, GaAs:Se, and GaAs:Zn has been carried out.

The technique of x-ray standing waves is a recent method for very accurate studies of surfaces and interfaces. Work on thin layers of Gadolinium Gallium Garnet crystal has been carried out at the AT&T Bell Laboratories. The apparatus for carrying out this technique with high resolution and reliability is now in operation at CNR. A project for the studies of adsorbates on crystalline surfaces is underway.

An experimental station with high angular resolution for x-ray standing waves and for Mossbauer Spectroscopy with synchrotron radiation is being put into operation at the Wiggler line of Adone in Frascati. The activity of epitaxial layers characterization is very important in connection with advanced growing techniques such as Molecular Beam Epitaxy and MOCVD. The CNR is collaborating with Centro Studi e Laboratori Telecommunicazioni (CSELT) on this subject.

Mossbauer Spectroscopy, in the transmission geometry, has been applied to the investigation of the magnetic phase of garnets and to the problem of distributing some ions among the different sites of the garnet structure. Furthermore, Mossbauer Spectroscopy has been applied to the investigation of the phase transformation Austenite-Martensite in some steels of technological interest.

Chemical Sensors

The activity at the CNR on sensors has dealt with basic devices that can allow the detection and quantitative analysis of gases including H_2, O_2, NH_3, and ions in solutions. The systems considered as testing vehicles for the fabrication of chemical sensors are:

- Metal oxide semiconductors (MOS) metal insulator semiconductors (MIS) structures
- Surface Acoustic Waves (SAW) structures
- Pyroelectric (Py) structures.

The MIS and MOS structures, using either silicon or amorphous silicon semiconductor material, are charge-responding devices that use a catalytic metal as gate electrode. When Pd is used, the MOS is sensitive to H_2 and shows a reversible response in the presence of O_2; I/V and C/V measurements are usually employed for the analysis of the responses. The SAW structures are mass responding devices. They have been designed and fabricated at CNR's Acoustic Institute and successfully tested at the Institute of Solid-State Electronics. By using Pd or Pt on the acoustical path of the devices, it is possible to get a remarkable sensitivity to H_2 and NH_3, respectively.

Py devices are sensitive to temperature variations occurring during a given catalytic reaction. A calibration of these devices has led to the determination of their thermal sensitivity of about 0.24×10^{-12} Kcal/cm^2/sec. Research on noise has also been active over the last 3 years to give a complete characterization of the above devices in operating conditions. Another important initiative was the production of thin films of A-Si, A-Si:H, and new insulators. The CNR is cooperating with a private research institution in the fabrication of chemical sensor-oriented devices.

Microwave Materials and Devices

Progressive refinement of the Liquid Phase Epitaxy technique over the last decade has allowed the reproducible growth of magnetic garnet films having a great variety of compositions. In particular, single crystal yttrium iron garnet ($Y_3Fe_5O_{12}$, [YIG]) epilayers characterized by low magnetic losses at microwave frequencies (commonly in the range 1-20GHz), have become available to develop planar devices based on the propagation of Magnetostatic Waves (MSW). The MSW-integrated devices and subsystems can play a significant role in such applications as dispersive and nondispersive delay lines, tunable filters and oscillators, pulse compressors, signal limiters and enhancers, convolvers, and correlators. The technologies available in the CNR have allowed the prototype fabrications (see Table 37).

The basic research on novel garnet compositions and propagation processes is active and is the source of interesting results, such as microwave solitons, which offer promise for further developments in applications. The above activity has been performed in cooperation with Selenia S.p.A. in radar and telecommunications. Selenia is the main user of the knowledge and devices. The CNR also cooperates with several American universities and institutions, mainly in magnetic propagation and electric properties of garnet films.

Table 37. CNR Prototype Fabrication

Dispersive delay line (DDL) tunable in the range 4-12GHz, with average delay time of the order of 150-200ns, -3dB bandwidth of 400-500 MHz, insertion loss of about 12-15dB
Nondispersive delay line obtained by cascading two DDLs through the frequency inversion of one of them (original patented technique) with the above characteristics
Oscillator tunable in the C and X band with high spectral purity comparable with or better than that of commercial YIB spheres oscillators (typically -100dBc/Hz at 10 kHz offset)
Tunable narrow bond filter obtained by using multilayered films alternating propagating (YIG) and absorbing (Ca-doped YIG) layers.

Biomagnetism

Biomagnetism is the study of magnetic signals associated with biological activity of functional areas of the human body. The detected signals are generated by intracellular bioelectric currents. Because the magnetic sensor is essentially an inductive coil positioned outside the body, the technique provides a unique, totally noninvasive means for directly investigating the biological activity. These signals are very weak and they always appear mixed with the environmental noise which is several orders of magnitude stronger. Only the development of superconducting quantum interference devices (SQUID) provided a magnetic sensor featuring a sensitivity adequate to the task. Various procedures have been proposed to reduce the ambient noise such as using heavily shielded electromagnetic rooms and rejecting fields originating relatively far from the magnetic sensor obtained by a particular geometry for the detection coil, which provides the spatial discrimination.

In Italy, activity in biomagnetism began 10 years ago at the CNR. A four-channel system has been operating for the last several years and it has enabled detection of magnetic fields simultaneously at four sites with sensitivities spanning around 40 ft/√Hz. Recent studies have concentrated on the brain. The magnetoencephalographic study of spontaneous brain activity is accomplished in collaboration with the Neurosurgery Institute of the University of Rome. A systematic investigation performed first on normal subjects, and later on pathological ones, has demonstrated that significant new information can be inferred from the magnetic analysis of cerebral activity. Through a systematic investigation of patients affected by various kinds of focal epilepsy, it has been demonstrated that the magnetic approach is powerful in the localization of the cortical areas responsible for the pathological activity.

Activity over the last several years has been carried out in collaboration with the neurophysiological groups of the University of Rome. The main goals of this work are to systematically compare the spatial distribution of the electric potentials and magnetic fields over the scalp of normal subjects and to identify common aspects and/or features which characterized only the magnetic approach. At present, a collaboration between the CNR and Elettronica S.p.A. is underway to develop a nine-channel system for neuromagnetic research. Finally, in cooperation with the CNR project on Superconductivity and Cryogenics, a *Class 100* system will be developed by 1991.

Electron Beam and X-ray Lithography

The CNR has been active in micron and submicron lithography since 1985. The main systems available are an electron beam microfabricator (Cambridge EBMF6) and deposition machines, including thermal evaporators and DC and RF magnetron sputtering for producing thin layers of insulators, metals, and amorphous semiconductors. A clean room is also available for processing prototype devices. There are seven main research themes at CNR (see Table 38).

The most important results (metallic patterns) obtained thus far by using both the Electron Beam Microfabricator (EBMF) and the lift-off techniques are:

- Micron region--A1 lines with line width of about 1μm and thickness greater than 6,000 Å
- Submicron region--An lines with line width of about 0.2μm and thickness around 100 Å
- Prototype of BN x-ray masks with fold-absorbing patterns (linewidth of about 0.2μm and thickness greater than 8,000 Å) achieved by EBMF and electroplating deposition.

The results are continuously transferred to the main electronic industry in Italy--SGS-Thomsom, Milan--which is a partner with the CNR in the National Microelectronics Program and the CNR project, *Materials and Devices for Solid State Electronics*.

The CNR recently began a program in mask technology and resist processes for x-ray lithography applications in submicron technology. The program is part of an ESPRIT project in which the CNR is prime contractor.

Table 38. CNR Main Research Themes

Apply the lift-off technique in the micron and submicron regions
Apply the electroplating deposition technique for x-ray mask fabrication
Study scattering and back scattering problems in electron beam lithography
Design and realize gates by the lift-off technique for GaAs MESFET and GaAs HEMT
Create micron and submicron sensors and cantilever structures for radiation sensitive devices
Fabricate optical and x-ray mask fabrication
Characterize devices.

Superconducting Devices

The study of DC-SQUIDs enables investigation of devices with noise near the quantum limit. The best devices are obtained with Josephson junctions with high-quality barriers. Thus, the study of various Josephson junctions is important in the research. Other devices studied are planar gradiometers and long Josephson junctions.

Investigations are underway in planar gradiometers for the future integration on a multichannel system; i.e., DC-SQUIDs and pickup coil, in gradiometer shape, integrated on the same chip. The DC-SQUIDs are also used in gravitational experiments carried out by the Rome group at CERN and in the future in the Gran Sasso underground laboratory. The CNR also plans to use DC-SQUIDs in experiments for detecting neutrinos and ULF signals from satellites. The CNR is also developing a fabrication process based on either direct writing on a silicon wafer by an EBMF or optical lithography using chromium masks generated by the EBMF. The thin-film technology is also used to pattern the various layers over the wafer. The process uses the lift-off technique on five out of the six layers (AuPd, NB_2O_5SiO, Niobium Oxide Barrier, and PbAnIn) while the first one (Nb) is obtained by reactive ion etching.

The CNR has a complete testing facility to study noise and the main physical properties of DC-SQUIDs and Josephson junctions at temperatures as low as 1K. They have developed an on-line data acquisition system and numerical simulation is used to study the dynamics of the devices. There is an on-going collaboration with an Italian electronics manufacturer to produce a 9-channel magnetometer system for use in biomagnetism.

High-Temperature Superconducting

In early 1987, the CNR obtained single phase sintered pellets of the high-temperature superconductor $YBa_2Cu_3O_{7-x}$, which exhibited a transition temperature of 93K with transition width of about 1K. Soon, work began on the possibility of getting single crystals of the new material to perform measurements of the compound's physical properties.[3] In May 1987, the CNR obtained the first single crystals in Italy, which were characterized in the laboratory, from the structural and from the electrical and magnetic viewpoints. The structural investigation was accomplished using a 0-20 x-ray diffractometer. The electrical resistivity was measured as a function of temperature using the 4-lead method. The AC magnetic susceptibility as a function of temperature was measured using a SQUID device of the change of inductance of a pick-up coil after the superconducting transition occurred. This is particularly useful in determining the transition temperature when the sample is too small to perform electrical resistivity measurements. Single crystals of $YBa_2Cu_3O_{7-x}$ about 4-mm wide have been obtained, with a transition temperature of about 85K. Some effort has been devoted to finding the most appropriate entectic of Ba and Cu in the flux method used to promote single crystal growth. Fabricating thin films of the new compound has begun. The facilities and the competence in the laboratory will be used to fabricate thin films and devices such as SQUIDs. In this work, collaboration with industry is very promising.

[3]Progress Report Consiglio Nazionale delli Ricerehe, Instituto de Elettronica dello Stato Solido, 1985-87, via Cinceto Romam, 42 00156 Roma, Italy.

Information Systems and Parallel Computing

Under the chairmanship of Professor C. Ciliberto, Chairman of the CNR Mathematical Science Committee, a proposal for a program on Information Systems and Parallel Computing was written and presented for government approval in early 1989. In June 1989, the program was approved and work began under CNR's sponsorship. The program will run for 5 years at an approximate cost of 9.4 billion lire/year (about $7.5 million/year).

The program goal is to carry out applied research in information systems and parallel computing by consortia of industrial and academic partners. The research areas include: Parallel Scientific Computing, Special Purpose Processors, Parallel Architectures, Future Generation Languages, Database Systems, Methods and Tools for System Design, and Systems in Support of Intellectual Activities. During the first year, the funds will be divided as follows:

- Parallel Scientific Computing - about 2.3 billion lire
- Special Purpose Processors - about 1.2 billion lire
- Parallel Architectures - about 1.2 billion lire
- Future Generation Languages - about 0.4 billion lire
- Database Systems - about 1.4 billion lire
- Methods and Tools - about 1.4 billion lire
- Systems and Support of Intellectual Activities - about 1.1 billion lire
- Other related expenses - about 0.4 billion lire.

Division of cost will be industrial partners - 44.71 percent, the academic community - 37.93 percent, and CNR - 17.36 percent. A summary of the work plan for the areas of the program are provided in the following paragraphs.

Parallel Scientific Computing

In the area of scientific computing, three fields will be considered:

1. Models and simulation will be accomplished on the application of large computer systems to general interest scientific problems, such as structural analysis and image processing, to acquire a better knowledge of some natural phenomena and to improve the design of high-technology products.

2. General purpose scientific software will consist of research in the field of fundamental parallel algorithms.

3. Mainframes access networks will provide access to mainframes in Italy, Europe, and the U.S., using high-speed connections and special workstations.

Special Purpose Processors

The three fields in this area are:

1. Coprocessors and modules will be used for image and signal processing

2. Coprocessors and modules for AI will include R&D of traditional chips, boards, and algorithms for implementing the most common functions of image and signal processing and AI.

3. Coprocessors and systolic modules will involve developing programable systolic systems under certain constraints such as temporization and cost.

Parallel Architectures

Computing systems seem to be moving towards more intensive use of parallelism, with architectures like single instruction stream, multiple data stream (SIMD), and MIMD. These architectures can support the logical and functional languages of AI.

A variety of matters to be considered in this connection include evaluating the performance of a parallel computing system, interconnecting the processors, and developing fault-tolerant strategies. In this area of parallel processors, the research will include multiprocessors, non-von Neuman architectures, and valuation and complexity.

Future Generation Languages

Developing new programing languages enhances support for new methods for processing data, including concurrency, distributed computing, and new data types. Also, the increased level of abstraction has made this field interesting from a logical viewpoint. Research in this area will cover logical, functional, and algebraic languages; concurrent and object-oriented languages; and interpreters, compilers, and runtime utilities.

Database Management Systems

The main goal in this area is to develop advanced user-oriented database management systems (see Table 39).

The following fields will be investigated: intelligent database systems, development of logical query languages, interaction with multimedia database, interaction with heterogeneous databases, and user-oriented methods and tools.

Table 39. CNR Database Management System Functions

Describe knowledge bases using advanced data models such as frames and rules
Interact with the database using logical languages
Interact with multimedia databases, with information including text, voice, and images
Interact with heterogeneous databases, with different databases connected via a network.

Methods and Tools for System Design

The design phase of a project is less automated since it is based on empirical methods, but it is the most delicate and important phase in a project. The aim of this research area is to develop specification systems and automatic tools to support the analysis and the design phase and to translate the specifications into code directly executable by the computer. The fields of investigation are cognitive engineering, specification systems, and prototypes.

Systems in Support of Intellectual Activities

The diffusion of the PC has led to the development of a large class of software packages for individual applications.

1. The decision support systems can be useful in all the situations where the estimation of the consequences of a certain decision are to be estimated. The aim is to develop tools that allow the user to construct his own decision support system.

2. The research in expert systems will lead to new design languages and new methods for the representation of knowledge.

3. In advanced individual productivity systems, new methods are being sought for the development of individual productivity tools.

Support Initiatives

In support of the research personnel, two support initiatives will be taken (see Table 40).

Table 40. CNR Support Initiatives

Parallel computing for organizing courses and state-of-the-art conferences in parallel computing and conducting performance analysis of commercial parallel and vector computers
Software engineering to build a library of standardized and unifying tools for software design and production.

Some Activities at the University of Pisa

Although the Parallel Processing and Computer Systems program only began in June 1989, I had discussions at the University of Pisa about the direction of their work and was given authors' abstracts of some previous work that will be relevant to their continued work on this program. The people with whom I talked at Pisa were Professor Piero Maestrini, Chairman, Faculty of Science; Professor Giorgio Gallo, Chairman, Computer Science Department; Professor Marco Vanneschi, Computer Science; and Professor Franco Turini, Computer Science.

Professor Vanneschi discussed plans to use both hardware; e.g., modifications of the T800 transputer, and software to achieve an optimal balance between computing and communicating in a parallel computer system. The necessary modifications in the T800 chip have not yet been determined but may include changes in the logic implemented on the chip to speed up communications and perhaps adding to the present four wires for input/output communication.

Professor Turini said that a major effort will be made on the combining of logic programing and functional programing into a single programing system. Logic programing appears to be best suited for the logical portions of an application, but it is weak for numerical computation. Functional programing will make its main contribution in the area of numerical computation.

Authors' abstracts of recent work that will be relevant to future work in the Parallel Processing and Computing Systems program is included herein.

Kernel LEAF: A Logic plus Functional Language, Elio Giovannetti et al. Kernel LEAF is a logic plus functional language based on the flattening technique, and differs from other similar languages in that it is able to cope with partial (undefined or nonterminating) functions. This is achieved by introducing the distinction between data structures and (functional) term structures, and by using two kinds of equality. The language has a clean model-theoretic semantics, where the domains of the interpretation are algebraic CPOs. In these domains, the difference between two equalities corresponds to a different behavior with respect to continuity. The operational semantics (based on SLD-resolution) is proved correct and complete with the model-theoretic one. Finally, an outermost strategy, more restrictive than SLD-resolution, but still complete, is presented.

Prolog as a Database Language, M. Eugenia Occhiuto and Renzo Orsini. A survey is presented of existing approaches to integrate Prolog and databases both at a linguistic and pragmatic level. All the proposals for integration become unsatisfactory because they result in the juxtaposition of two very different languages, or because they cannot offer adequate mechanisms to deal with persistent data. This paper indicates the critical issues of such integration to overcome some of the limitations of the proposed systems and to support the design of future integrated systems.

The Concurrent Language Shared Prolog, Antonio Brogi and Paolo Ciancarini. This paper introduces the concurrent logic language Shared Prolog (SP). An SP is composed of a set of modules that are Prolog programs extended by a guard mechanism coordinating communication and synchronization via a centralized data structure. This communication system is inherited from the blackboard model of problem solving. Intuitively, the granularity of the processes to be elaborated in parallel is large, while the resources shared on the blackboard have a very small granularity (they are Prolog facts). An operational semantics is given in terms of a partial ordering, distributed model. The expressiveness of the language is shown with respect to the specification of two possible classes of applications--software engineering environments and expert systems.

Cost and Process Mapping in Massively Parallel Systems: A Static Approach, Silvano Antonelli et al. An integrated approach to the mapping of processes of a concurrent program onto processing nodes of a massively parallel system is presented. Only general purpose systems in the microcomputer array class, and hence with a regular communication structure, are considered. No constraints are imposed on the communication structure of the program to be mapped but, since process mapping is solved during compilation, the proposed solution may be applied only to programs whose structure is statically derivable.

The mapping is implemented in two steps. In step one, an undirected, weighted graph describing process communications is built starting from the concurrent program to be mapped. The weight of an edge expresses the amount of data exchanged between a pair of processes, and is determined using only structural characteristics of the program. A detailed heuristic algorithm for an estimation of the weights is described. This step is fundamental for the definition of a programing tool implementing process mapping.

During step two, the nodes of the graph are mapped onto system nodes. The goal of the mapping is to reduce the cost of interprocess communications without reducing actual parallelism among processes. Since the problem is NP-hard, an heuristic algorithm has been developed to approximate the optimal mapping. The performance of the whole approach, cost evaluation, and mapping is discussed through a set of examples.

A Declarative Approach to Abstract Interpretation of Logic Programs, Robert Barbuti et al. The theory of Abstract Interpretation provides a formal framework to develop advanced dataflow analysis tools for logic programing. The idea is to define a nonstandard semantics which is able to compute, in finite time, an approximated model for the program. In the present paper, we define an abstract interpretation framework based on the standard fixpoint approach to the semantics. This leads to the definition, by means of a set of operators, of an abstract declarative semantics, which returns an abstract fixpoint characterization of the minimal Herbrand model associated with the program. Thus, we obtain a specializable abstract framework for bottom-up abstract interpretations of logic programs.

Algebraic Structures and Completion for Higher Order Logic Programs, Roberto Barbuti et al. In this paper, we extend to a higher order logic programing language some relevant results of the classical first-order logic programing paradigm. First, we adapt to this ambit the notions of success and failure sets, and we show some interesting computational characterizations of a higher order logic program. Then we consider a *Negation as Failure* (n.a.f.) approach to negation and we give a notion of completion for higher order logic programs and a model-theoretic characterization of n.a.f., analogous to those introduced by Clark. In particular, we show the soundness and completeness of n.a.f. with respect to completion. Finally, we describe an algebra of higher order logic programs, which is the first step to the construction of a modular structure that maintains a clear semantics and a declarative reading.

Formal Theories of Inheritance for Typed Functional Languages, Roberto Amadio. An interesting model-theoretic notion of inheritance arises when working in realizability structures. The purpose of this paper is to define formal theories of inheritance, inspired by the models, and to stress their relevance by completeness theorems and an analysis of the proof-theoretic properties. Towards this aim, we consider a relatively simple language, namely a second order lambda-calculus with records and recursive types. This choice allows an explanation at an elementary level of the main mathematical and methodological issues.

Participation in European Programs

ESPRIT

Italy has been the fourth most active participant in ESPRIT, after the U.K., France, and FRG. Italy had 45 companies and 10 universities as participants in ESPRIT I. Italy continues to be active in ESPRIT II.

EUREKA

Italy is active in about 28 percent of EUREKA projects.

RACE

During the RACE Definition Phase, which was completed in 35 different sectors of R&D, Italy had companies in 15 of these sectors; in one case, five companies participated.

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